White Paper 3
System Level ESD
Part II: Implementation of Effective ESD Robust Designs

Industry Council on ESD Target Levels

September 2012

Revision 1.0

This document is available through various public domains as listed below:

The Industry Council on ESD
http://www.esdindustrycouncil.org/ic/en/

The Electrostatic Discharge Association
http://www.esda.org/

JEDEC – Under Publication JEP162
http://www.jedec.org/

Abstract

This document (White Paper 3 Part II) is the second of two Electrostatic Discharge (ESD) Industry Council white papers dealing with System Level ESD.

In Part I, the misconceptions common in the understanding of system level ESD between supplier and original equipment manufacturer (OEM) were identified, and a novel ESD component / system co-design approach called system efficient ESD design (SEED) was described. The SEED approach is a comprehensive ESD design strategy for system interfaces to prevent hard (permanent) failures. In Part II we expand this comprehensive analysis of system ESD understanding to categorize all known system ESD failure types, and describe new detection techniques, models, and improvements in design for system robustness. Part II also expands this SEED co-design approach to include additional hard / soft failure cases internal to the system.

Part II begins with an overview of system ESD stress application methods and introduces new system diagnosis methods to detect weak ESD failure areas leading to hard or soft failures, and provides a "cost vs. performance vs. robustness" analysis of present-day state-of-the-art EMC/EMI design prevention methods that have been developed to prevent system level ESD failure. It follows with an expansion of SEED failure classifications to cover a combination of hard (permanent) and/or soft (resettable) system failures and stresses which could cause these errors, and describes cases where the SEED co-design approach can be expanded to provide additional benefits to system ESD design. System design simulation tools are described in the context of their potential improvements to simulating system level ESD stress and failure modes. Application-specific industry system ESD test methods are then described in the context of their ability to reveal hard and soft failure modes from actual system deployment. Finally, a technology roadmap of the system design components is described, including IC technology and related circuit speeds, automotive electronics, packaging technology, system / board interconnect technology and ESD protection materials, illustrating continuing challenges for system ESD design improvement.

About the Industry Council on ESD Target Levels

The Council was initiated in 2006 after several major U.S., European, and Asian semiconductor companies joined to determine and recommend ESD target levels. The Council now consists of representatives from active full member companies and numerous associate members from various support companies. The total membership represents IC suppliers, contract manufacturers (CMs), electronic system manufacturers, OEMs, ESD tester manufacturers, ESD consultants and ESD IP companies. In terms of semiconductor market leaders, the member IC manufacturing companies represent 8 of the top 10 companies, and 12 of the top 20 companies as reported in the EE Times issue of November 9, 2010.

Core Contributing Members	**Core Contributing Members**
Robert Ashton, ON Semiconductor	Guido Notermans, ST-Ericsson
Jon Barth, Barth Electronics	Nate Peachey, RFMD
Patrice Besse, Freescale	Ghery Pettit, Intel
Stephane Bertonnaud, Texas Instruments	David Pommereneke, Missouri University of Science & Technology
Brett Carn, Intel Corporation	Wolfgang Reinprecht, AustriaMicroSystems
Ann Concannon, Texas Instruments	Alan Righter, Analog Devices
Jeff Dunnihoo, Pragma Design	Theo Smedes, NXP Semiconductors
Charvaka Duvvury, Texas Instruments (Chairman) c-duvvury@ti.com	Teruo Suzuki, Fujitsu
	Pasi Tamminen, Nokia (* - Advisory board also)
David Eppes, AMD	Matti Uusimaki, Nokia
Howard Gan, SMIC	Benjamin Van Camp, SOFICS
Reinhold Gärtner, Infineon Technologies	Vesselin Vassilev, Novoroll
Robert Gauthier, IBM	Terry Welsher, Dangelmayer Associates
Horst Gieser, FhG IZM	Joost Willemen, Infineon Technologies
Harald Gossner, Intel Corporation (Chairman) harald.gossner@intel.com	
	Advisory Board*
LeoG Henry, ESD/TLP Consulting	Fred Bahrenburg, Dell
Masamitsu Honda, Impulse Physics Laboratory	Heiko Dudek, Cadence
Michael Hopkins, Amber Precision Instruments	Bob Dutton, Stanford University
Hiroyasu Ishizuka, Renesas Technology	Johannes Edenhofer, Continental
Satoshi Isofuku, Tokyo Electronics Trading	Stephen Frei, Technical University of Dortmund
Marty Johnson, National Semiconductor	Frederic Lefon, Valeo
John Kinnear, IBM	Christian Lippert, Audi
David Klein, Freescale Semiconductor	Patrice Pelissou, EADS
Timothy Maloney, Intel Corporation	Wolfgang Pfaff, Bosch
Tom Meuse, Thermo Fisher Scientific	Tuomas Reinvuo, Nokia
James Miller, Freescale Semiconductor	Marc Sevoz, EADS
	Werner Storbeck, Volkswagen
	Wolfgang Wilkening, Bosch
	Rick Wong, Cisco

Associate Members	**Associate Members**
Stephen Beebe, Global Foundries	Soon-Jae Kwon, Samsung
Jonathan Brodsky, Texas Instruments	Brian Langley , ORACLE
Michael Chaine, Micron Technology	Frederic Lafon, Valeo
Freon Chen, VIA Technologies	Moon Lee, SemTech
Tim Cheung, RIM	Markus Mergens, QPX
Ted Dangelmayer, Dangelmayer Associates	Roger Peirce, Simco
Ramon del Carmen, Amkor	Donna Robinson-Hahn, Fairchild Semiconductor
Stephanie Dournelle, ST Microelectronics	Jeff Salisbury, Flextronics
Melanie Etherton, Freescale Semiconductor	Jay Skolnik, Skolnik-Tech
Yasuhiro Fukuda, OKI Engineering	Jeremy Smallwood, Electrostatic Solutions Inc.
Kelvin Hsueh, UMC	Jeremy Smith, Silicon Labs
Natarajan Mahadeva Iyer, Global Foundries	Arnold Steinman, Electronics Workshop
Larry Johnson, LSI Corporation	David E. Swenson, Affinity Static Control Consulting
Peter de Jong, Synopsys	Nobuyuki Wakai, Toshiba
Jae-Hyok Ko, Samsung	Jon Williamson, IDT
ChangSu Kim, Samsung	Michael Wu, TSMC
Han-Gu Kim, Samsung	MyoungJu.Yu, Amkor
Marcus Koh, Everfeed	

Acknowledgments:

The Industry Council would like to thank all the authors, reviewers, and specialists who shared a great deal of their expertise, time, and dedication to complete this document. The authors of Appendix B would like to thank several individuals for their insight into the future roadmap, Chris Barr (TI) and Christopher Opoczynski (TI) for projections on universal serial bus (USB) and high definition multimedia interface (HDMI) and Andrew Marshall (TI) for an overview on optical interconnects. Wolfgang Stadler (Intel) is acknowledged for his contributions to the transient latch-up discussion in Chapter 4. We would especially like to thank our OEM advisors from Audi, Bosch, Cadence, Continental, Cisco, Dell, EADS, Nokia, Technical University of Dortmund, Valeo and Volkswagen who gave us valuable direction. The Industry Council would also like to thank the Electrostatic Discharge Association (ESDA) for facilitating the face-to-face meetings of the Council.

Editors:
Brett Carn, Intel Corporation
Terry Welsher, Dangelmayer Associates

Authors:
Robert Ashton, ON Semiconductor
Jon Barth, Barth Electronics
Patrice Besse, Freescale Semiconductor
Jeff Dunnihoo, Pragma Designs, Inc
Charvaka Duvvury, Texas Instruments
David Eppes, AMD
Harald Gossner, Intel Corporation
Leo G. Henry, ESD/TLP Consulting
Masamitsu Honda, Impulse Physics Laboratory
Mike Hopkins, Amber Precision Instruments
Marty Johnson, Texas Instruments
David Johnsson, Intel Corporation
David Klein, Freescale Semiconductor
Tom Meuse, Thermo Fischer Scientific
Tim Maloney, Intel Corporation
Guido Notermans, ST-Ericsson
Ghery Pettit, Intel Corporation
David Pommerenke, Missouri University of Science & Technology
Alan Righter, Analog Devices
Wolfgang Reinprecht, Austria Microsystems
Pasi Tamminen, Nokia
Matti Uusimaki, Nokia
Benjamin Van Camp, SOFICS
Vesselin Vassilev, Novorell
Joost Willemen, Infineon Technologies

Mission Statement

The Industry Council on ESD Target Levels was founded on its original mission to review the ESD robustness requirements of modern IC products to allow safe handling and mounting in an ESD protected area. While accommodating both the capability of the manufacturing sites and the constraints posed by downscaled process technologies on practical protection designs, the Council provides a consolidated recommendation for future ESD target levels. The Council Members and Associates promote these recommended targets for adoption as company goals. Being an independent institution, the Council presents the results and supportive data to all interested standardization bodies.

In response to the growing prevalence of system level ESD issues, the Council has now expanded its mission to directly address one of the most critical underlying problems: insufficient communication and coordination between system designers (OEMs) and their IC providers. A key goal is to demonstrate and widely communicate that future success in building ESD robust systems will depend on adopting a consolidated approach to system level ESD design. To ensure a broad range of perspectives the Council has expanded its roster of Members and Associates to include OEMs as well as experts in system level ESD design and test.

Preface

While IC level ESD design and the necessary protection levels are well understood, system ESD protection strategy and design efficiency have only been dealt with in an ad hoc manner. This is most obvious when we realize that a consolidated approach to system level ESD design between system manufacturers and chip suppliers has been rare. This White Paper discusses these issues in the open for the first time, and offers new and relevant insight for the development of efficient system level ESD design. This effort has been divided into two parts. In WP3 Part I, we identified the misconceptions common in the understanding of system level ESD. In this document (Part II) we will explore realistic system ESD protection requirements and strategies. We would also like to note that in Part I we addressed direct stress effects on external and internal pins of an IC while this document investigates the intricate effects of inter-chip pin coupling. This document is intended to be useful for both chip suppliers and OEMs/ODMs. As a final note, we would like to clarify that this document addresses system level ESD issues only, not electrical overstress (EOS) issues unless they manifest from a system failure.

Disclaimers

The Industry Council on ESD Target Levels is not affiliated with any standardization body and is not a working group associated with JEDEC, ESDA, JEITA, IEC, or AEC.

This document was compiled by recognized ESD experts from numerous semiconductor supplier companies, contract manufacturers and OEMs. The data represents information collected for the specific analysis presented here; no specific components or systems are identified.

The Industry Council, while providing this information, does not assume any liability or obligations for parties who do not follow proper ESD control measures.

Table of Contents

Glossary of Terms 11
Definitions 14
Executive Summary 16
Chapter 1: Introduction & Purpose 20
1.0 History of the Industry Council on ESD Target Levels 20
1.1 White Paper 3 Part II: Summary of Chapters/Appendices 21
Chapter 2: Overview of ESD Stressing and System Response 24
2.0 Introduction 24
2.1 Presently Used Stress Tests for ESD 24
2.2 Definitions 25
2.3 Coupling of ESD into Systems and Circuits 26
2.4 Troubleshooting to Determine the Cause of Failures 30
2.5 New Technologies for Determining Root Cause of Failures 31
2.6 Summary 34
Chapter 3: State-of-the-Art ESD/EMI Co-design 35
3.0 Introduction 35
3.1 The Basics 37
3.2 Advanced System ESD Protection Methods 44
3.3 Comprehensive Co-Design Methodologies 51
3.4 Conclusion 51
Chapter 4: Reference Methodologies for IC/System Protection Co-Design 53
4.0 Introduction 53
4.1 Approaches – Categories 55
4.2 Examples 65
Chapter 5: Standard Model and Analytical Tool Needs To Support SEED 73
5.0 Introduction 73
5.1 Component Characterization and Model Requirements to Support SEED Category 1 74
5.2 Component Characterization and Model Requirements to Support SEED Category 2 83
5.3 System Characterization and Model Requirements to Support SEED Category 3 84
5.4 Conclusion 93
Chapter 6: Summary and Conclusions 96
6.0 Introduction 96
6.1 Overview of ESD Stressing and System Response - Chapter 2 96
6.2 State-of-the-Art ESD/EMI Co-Design - Chapter 3 97
6.3 Reference Methodologies for IC/System - Chapter 4 98
6.4 Standard Model and Analytical Tool Needs to Support SEED - Chapter 5 99
6.5 Application Specific Information on System ESD Related Tests and Their Targets – Appendix A 100
6.6 Technology Roadmap and Direction – Appendix B 100
6.7 Outlook 102
Appendix A: Application Specific Information on System ESD related Tests and their Targets 103
A.0 Introduction 103
A.1 System Tests and Targets of Mobile Phones 103
A.2 System Tests and Targets of Automotive Electronic Components 105
A.3 System Tests and Targets of Computing Devices 108
A.4 System Tests and Targets of Medical Electronic Components 108
A.5 System Tests and Targets of Avionic Components 110
A.6 System Tests and Targets of Consumer Electronic Devices 111
A.7 Applicability of System-Efficient ESD Design (SEED) 112
Appendix B: Technology Roadmap and Direction 116
B.0 Introduction 116
B.1 Roadmap for ICs: Microprocessors 117
B.2 Roadmap for Automotive Applications 120
B.3 Roadmap for IC Package and Applications 121
B.4 Advances in Board and Assembly Technologies 123
B.5 Optical Interconnects 126

B.6 Polymer Applications....127
B.7 Future Compatibility to IEC Protection Requirements....128
Appendix C: Fast and Slow ESD Stress (High and Low Frequency Spectrum)....133
C.0: Discussion....133
C.1: Some Words on ESD Debugging....136
Appendix D: Review of White Paper 3 Part I....137
D.1 Part I Chapter 1: Purpose and Introduction....137
D.2 Part I Chapter 2: Test Methods and Their Field of Application....137
D.3 Part I Chapter 3: Proven System Level Fails....139
D.4 Part I Chapter 4: OEM System Level ESD Needs and Expectations....140
D.5 Part I Chapter 5: Lack of Correlation between HBM/CDM and IEC 61000-4-2....141
D.6 Part I Chapter 6: Relationship between IC Protection Design and System Robustness....142
D.7 Part I Chapter 7: Summary, Conclusions and Outlook....144
Appendix E: Frequently Asked Questions....146
Revision History....153

Glossary of Terms

AAMI	Association for the Advancement of Medical Instrumentation
AC	alternating current
ADC	analog digital converter
AEC	Automotive Electronics Council
AMR	absolute maximum rating
ANSI	American National Standards Institute
ASIC	application specific integrated circuit
ASTM	American Society for Testing and Materials
ATE	automated test equipment
BCD	bipolar-CMOS-DMOS
BOM	bill of materials
CAD	computer aided design
CAN	controller area network
CBE	charged board event
CCL	capacitive coupled latch-up
CDE	cable discharge event
CDM	charged-device model
CISPR	Comité International Spécial des Perturbations Radioélectriques
CMOS	complimentary metal-oxide-semiconductor
CMF	common mode filter
CRC	cyclic redundancy check
DC	direct current
DDR	double data rate
DIP	dual inline package
DMOS	double-diffused metal-oxide-semiconductor
DSP	digital signal processing
DVI	digital visual interface
DUT	device under test
ECU	electronic control unit
EDA	electronic design automation
EEPROM	electrically erasable programmable read only memory
EFT	electrical fast transients
EM	electromagnetic
EMMI	emission microscopy
EOS	electrical overstress
ESD	electrostatic discharge
ESDA	Electrostatic Discharge Association; ESD Association
ETSI	European Telecommunication Standards Institute
EUT	equipment under test
FB	ferrite bead
FDA	Food and Drug Administration
FET	field effect transistor
FFT	fast Fourier transform
GND	negative voltage supply in digital logic, neutral voltage supply in analog logic
GPIO	general purpose input/output

HBM	human body model
HDL	hardware description language
HDMI	high definition multimedia interface
HMM	human metal model
IBIS	input/output buffer information specification
IC	integrated circuit
ID	identification
IO	input/output
IEC	International Electrotechnical Commission
IR	infra-red
ISO	International Organization of Standards
IT	information technology
ITE	information technology equipment
I-V	current/voltage
JEDEC	Joint Electronic Devices Engineering Council
JEITA	Japan Electronics and Information Technology Industries Association
JTAG	joint test action group
LCD	liquid crystal display
LED	light emitting diode
LIN	local interconnect network
MCM	multi-chip module
MDD	medical device directive
MEM	micro-electro-mechanical
MID	molded interconnection device
MM	machine model
OEM	original equipment manufacturer
ODM	original design manufacturer
OTP	one time programmable
PC	personal computer
PCB	printed circuit board
PCI	peripheral component interconnect
PHY	physical layer interface
PLL	phase lock loop
PN	p-type/n-type junction
PWB	printed wiring board
R2R	roll-to-roll
RAM	random access memory
RC	resistor capacitor network
RF	radio frequency
RLC	resistor inductor capacitor network
RTOS	real time operating system
RX	receiver
SAE	Society of Automotive Engineers
SAW	surface acoustical wave
SCR	silicon controlled rectifier
SERDES	serializer/deserializer
SIM	subscriber identity module
SiP	system-in-package

SMA	sub-miniature version A
SMT	surface mount technology
SOA	safe operating area
SoC	system-on-chip
SoP	system-on-package
SP	standard practice
SPD	surge protected device
SPICE	simulation program with integrated circuit emphasis
TCAD	technology computer-aided design
TIVA	thermally induced voltage alteration
TLP	transmission line pulse
TLU	transient latch-up
TSV	through silicon via
TV	television
TVS	transient voltage suppression
TX	transmitter
USB	universal serial bus
UV	ultra violet
VDD	positive voltage supply
VFTLP	very fast transmission line pulse
VHDL	Verilog hardware description language
VSS	negative voltage supply
WP	white paper
WSP	wafer scale package
XTAL	crystal oscillator

Definitions

Crosstalk: Any phenomenon by which a signal transmitted on one circuit or channel of a transmission system creates an undesired effect in another circuit or channel. This phenomenon is usually caused by undesired capacitive, inductive, or conductive coupling from one circuit, part of a circuit, or channel, to another.

EMC: electromagnetic compatibility – The condition which prevails when telecommunications (communication-electronic) equipment is collectively performing its individual designed functions in a common electromagnetic environment without causing or suffering unacceptable degradation due to electromagnetic interference to or from other equipment/systems in the same environment (MIL-STD-463A).

EMI: electromagnetic interference - Electromagnetic emissions (radiated or conducted) which may cause harmful interference to communications services or other electronic devices.

ESD Design Window: The ESD protection design space for meeting a specific ESD target level while maintaining the required IO performance parameters (such as leakage, capacitance, noise, etc.) at each subsequent advanced technology node.

External Pin (interface pin): An external pin is one which at the board/card level is exposed to potential ESD threats from the outside world.

FR-4 (or FR4): A grade designation assigned to glass-reinforced epoxy laminate sheets, tubes, rods and printed circuit boards.

Hard Failure: Failure of a system due to physical damage to a system component which can only be repaired by the physical repair or replacement of the damaged component.

IEC-Robustness: The capability of a product to withstand the required IEC ESD-specification tests and still be fully functional.

IEC ESD event: An ESD stress as defined in IEC 61000-4-2.

Immunity: The ability of an electronic device to function properly in its electromagnetic environment.

Internal Pin (non-interface pin): An internal pin is one which is exposed to ESD threats typically only during IC manufacturing or during a crosstalk situation at the system level.

Residual Pulse: The resulting voltage/current (after system level ESD protection devices) seen by an IC component from an IEC stress waveform.

Second breakdown trigger current - I_{t2}: The current point at which a transistor enters its second breakdown region under ESD pulse conditions and is irreversibly damaged.

SEED: System-Efficient ESD Design - Co-design methodology of on-board and on-chip ESD protection to achieve system level ESD robustness.

Susceptibility, conducted: A measure of the interference signal current or voltage required on power, control and signal leads to cause an undesirable response or degradation of performance (MIL-STD-463A).

Susceptibility, electromagnetic: The degree to which an equipment, subsystem or system evidences undesired responses caused by electromagnetic radiation to which it is exposed (MIL-STD-463A).

Susceptibility, radiated: A measure of the radiated interference field required to cause equipment degradation (MIL-STD-463A).

Susceptibility threshold: The signal level at which the test sample exhibits a minimum discernible undesirable response (MIL-STD-463A).

System level ESD Robustness: The capability of a product to withstand the required IEC ESD-specification tests and still be fully functional.

Soft Failure: Failure of a system, not due to physical damage, in which the system can be returned to a functional state without the repair or replacement of a component. Return to a functional state may or may not require operator intervention. Operator intervention may include rebooting or power cycling. Soft Failures can involve software issues and software fixes but in the context of this document they are primarily due to ESD events injecting unwanted signals into the system which place the system into a state in which it does not function as intended.

VHDL-AMS: Verilog-AMS is a derivative of the Verilog hardware description language. It includes analog and mixed-signal extensions (AMS) in order to define the behavior of analog and mixed-signal systems. It extends the event-based simulator loops of Verilog / System Verilog / VHDL, by a continuous-time simulator, which solves the differential equations in analog-domain. Both domains are coupled: analog events can trigger digital actions and vice versa.

Executive Summary

Overview

White Paper 3 Part II, while establishing the complex nature of system level ESD, proposes that an **efficient ESD design can only be achieved when the interaction of the various components under ESD conditions are analyzed at the system level**. This objective requires an appropriate characterization of the components and a methodology to assess the entire system using simulation data. This is applicable to system failures of different categories (such as hard, soft, and electromagnetic interference (EMI)). This type of systematic approach is long overdue and represents an advanced design approach which replaces the misconception, as discussed in detail in White Paper 3 Part I, that a system will be sufficiently robust if all components exceed a certain ESD level.

In the first step, a method for categorizing the failure types has been introduced. An advanced characterization and simulation approach is discussed through examples. However, a full design flow cannot be established without **a common effort across the electronic industry involving IC suppliers, suppliers of discrete protection components and original equipment manufacturers (OEMs) as well as tool vendors**. This paper identifies existing tools with both simulations and scanning techniques that are applicable for this purpose and calls out fields for further development.

Equally important is the notion that **efficient system ESD design can ideally be achieved by improved communication between the IC supplier, the OEM and the system builder**. As technologies advance even further, and as systems become more complex under various applications, this shared responsibility is expected to gradually shift more towards system design expertise.

Understanding Component to System ESD

Towards achieving the goals mentioned above, it is first important to decouple the component ESD requirements from system level ESD design. White Papers 1 and 2 established that component electrostatic discharge (ESD) levels can be safely reduced to practical levels with basic ESD control methods that are mandatory in every production area. We have also established that these ESD target levels enable fabrication of integrated circuits (ICs) with on-time delivery (in billions of units) for electronic systems in consumer applications with high circuit performance. The general perception has been that component ESD (for example, human body model (HBM)) is a prerequisite for good system level ESD robustness. But this misconception once again needs to be clarified, as shown below in Figure 1, **system level ESD and component ESD are not correlated with each other.**

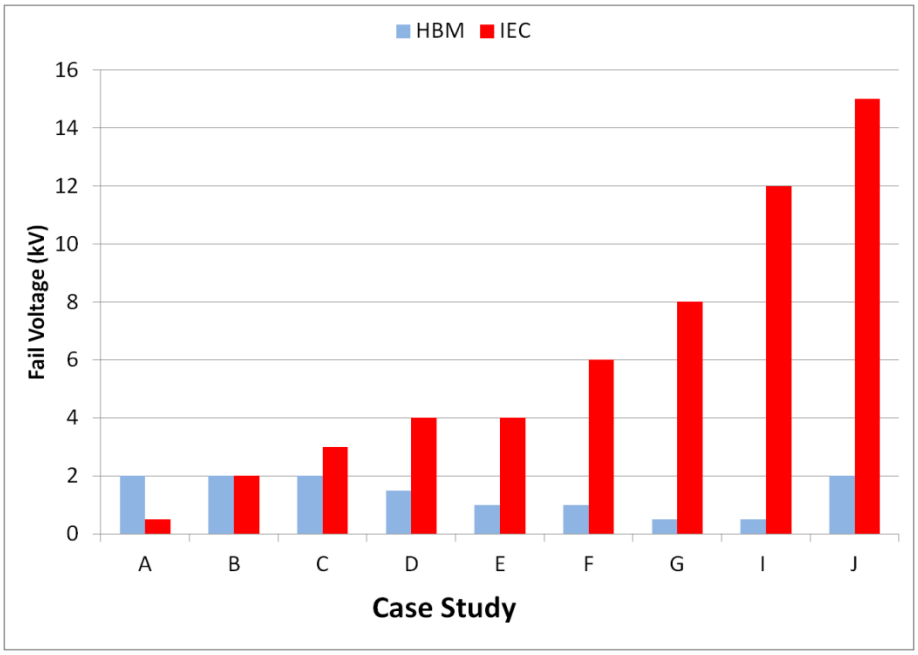


Figure 1: Comparison of IC level and system level ESD failure threshold of various systems (A-J) showing that HBM protection is not related to System level ESD robustness

In fact, at the system level, ESD robustness is a much more complex issue requiring a deeper understanding to address the ESD protection requirements for electronic systems such as laptops, cell phones, printers and home computers. These system complexities come about as a result of protecting the external interfaces, such as the universal serial bus (USB), to the outside world. Such systems, after encountering the more severe ESD pulses defined by the IEC standard, can lead to hard or soft failures. As introduced in White Paper 3 Part I, the basic version of system-efficient ESD design (SEED) addresses **hard failures** related to IC pins with a direct external interface, **soft failures,** which are more frequently reported, are challenging to understand and overcome. In this latter case, addressing soft failures requires an extension of the SEED approach to other failure mechanisms that include latch-up and EMI effects. In this document, the steps to categorize the different failure mechanisms, and the appropriate characterization and simulation methodologies, are identified through various forms of **Advanced SEED**.

Communication and Strategy

This white paper documents a rigorous approach to describing **the challenges related to all categories of system level ESD failures** that can arise from energy injection due to the IEC contact pulse stress, as well as from electromagnetic compatibility (EMC) and EMI effects. To classify these fails and to provide a common terminology, three categories of fails have been introduced:

- SEED Category 1 (physical damage due to pulse energy)
- SEED Category 2 (damage or interference of function due to transient latch-up)
- SEED Category 3 (interference of function by noise or bursts on supply net and signal lines)

Understanding these different categories of failures is an important part of addressing the appropriate solutions. Thus, one main objective is to close the existing communication gap between OEMs and IC providers by involving the expertise of both OEMs and system design experts. As a result, the completion of this second phase of White Paper 3 required the participation and contributions from world class experts on the art of system level ESD phenomena and protection techniques.

One of the challenges which remains elusive is the trade-off between cost, performance, robustness, and time-to-market. This white paper also addresses these issues, bringing forth a dialogue between the IC supplier, customer, and the system designer.

Implementation of Advanced Tools

White Paper 3 Part II specifically covers in detail **an overview of system ESD stress application methods, system diagnostic techniques to detect hard or soft failures, and the application of tools for susceptibility scanning.** For example, as illustrated in Figure 2, these types of advanced tools can be used to differentiate the characteristics of products and enable proper system protection methodology.

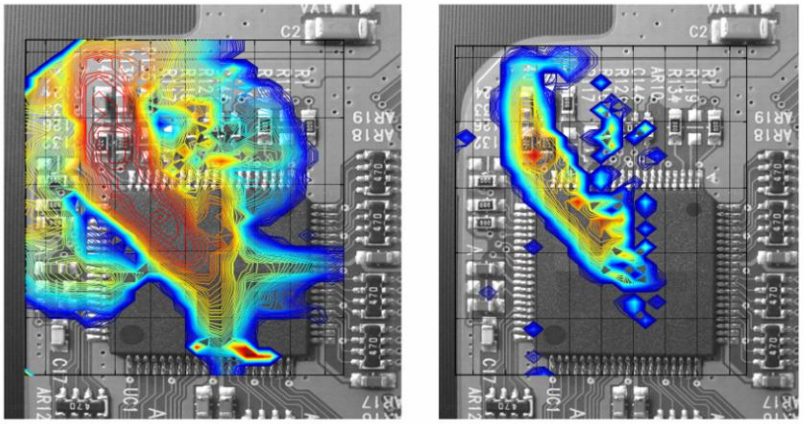


Figure 2: Susceptibility scanning using pulse techniques on Product A (left) and Product B (right)
(Courtesy of Amber Precision Instruments)

Along the lines of communication and interaction, IC suppliers and system designers can share their knowledge of tools and their applications. For example, suppliers would provide a single definition, high quality model of their input/output (IO). Then OEMs would use analytical tools to integrate the IC's IO models into their system models for system level stress analysis. These tools will not reach their full potential unless the data they collect can be used within the standard design flow for an electronic system. For these to be effective, model files such as input/output buffer information specification (IBIS) and simulation programs with integrated circuit emphasis (SPICE), which describe the electrical properties of components, need to be enhanced to describe component behavior in the ESD range. Suppliers of components, ranging from integrated circuits to ESD protection components also need to characterize their products in the appropriate ESD range.

Impact from the Technology Roadmap

Finally, we bring into focus that IC technology and related circuit speeds will increasingly have an impact on system designs. This roadmap will cover market segments ranging from information technology (IT), communications, automotive electronics, IC package technology development to advances in board and assembly technologies. **The cost of ESD must be considered along with all development and innovation; the industry must decide who should bear the cost of ESD design and its pressure on production schedules and time to market**

System level ESD will continue to be a challenge in the future. The dilemma of meeting technology demands for speed and performance will inevitably require either the development of more effective shielding or innovation of novel on-board protection solutions.

Conclusions

In summary, this white paper has pointed out the necessary framework required for comprehensive improvement in the first time success rate of ESD robust system designs. A number of helpful tools and techniques already exist. However, standardization between IC suppliers, PCB protection device suppliers and system designers requires common models, common methods and compatible simulation tools in order to meet the goal of better ESD design capability. **None of this will occur without a great deal of communication between EDA tool vendors, component suppliers and system designers.**

Finally, this document has provided a major step forward in identifying and understanding the technical issues. An important message to remember is that **the current focus on component ESD performance must shift towards improving system level ESD performance. That is, while minimum component ESD levels provide for safe component handling, the bulk of future research and development efforts should be directed towards system level ESD to reach a day when a high first pass success rate in system level ESD design is straightforward.**

Chapter 1: Introduction & Purpose

Robert Ashton, ON Semiconductor
Charvaka Duvvury, Texas Instruments

1.0 History of the Industry Council on ESD Target Levels

The Industry Council on ESD Target Levels (Council) was formed in 2006 to address a growing disconnect between original equipment manufacturers (OEMs) and manufacturers of integrated circuits (ICs) with regard to electrostatic discharge (ESD). The competitive environment requires that OEMs create products with higher performance in ever smaller form factors while maintaining and improving reliability and offering the products at competitive prices. This progress was made possible by imposing the following improvements in ICs; higher levels of functionality, higher speeds, smaller component size and lower power. That is, the burden of higher performance has been transferred to the IC suppliers, who must achieve these improvements through enhancements in their chip designs. IC manufacturers have been able to make these improvements by employing new IC technologies with smaller feature sizes to improve functionality and speed and lower working voltages to prevent wear-out of the circuit and maintain reasonable power levels.

OEMs of course need these improvements, but they do not want them at the cost of reliability and yield. OEMs therefore maintained the same quality and reliability requirements on ICs produced in the latest technology as they had for a more mature product. One of these requirements was for the ESD robustness of ICs. 2 kV of human body model (HBM) robustness had long been a *de facto* standard and 500 V of charged device model (CDM) robustness was becoming a similar requirement. Also, there was an unintended, albeit perceived important, requirement that the ICs must simultaneously meet 200 V for the machine model (MM). However, starting around the 90 nm technology node, IC manufacturers were finding it increasingly difficult, and sometimes impossible, to consistently meet these requirements. The smaller feature sizes, lower operating voltages and high speed signal requirements of ICs were shrinking the design window available for ESD protection. IC manufacturers, however, knew that 2 kV HBM and 500 V CDM levels were not needed. HBM and CDM tests are performed to ensure that ICs can survive manufacture in an ESD controlled manufacturing facility. Experience has shown that with basic ESD control procedures, ICs with far lower HBM and CDM levels could be handled. Furthermore, without basic ESD controls, robustness far beyond 2 kV HBM and 500 V CDM will not survive. Attempting to meet 2 kV HBM and 500 V CDM was therefore costing the industry millions of dollars in redesigns and delays to market without any benefit to the industry.

The Council was formed to show the electronics industry that lowering ESD levels from 2000 V HBM and 500 V CDM was not only possible without sacrificing quality and reliability, but also the right thing to do. “White Paper 1: A Case for Lowering Component Level HBM/MM ESD Specifications and Requirements” [1] demonstrated why it was becoming more difficult to design high levels of HBM performance in advanced technologies and presented data that proved lower HBM levels do not lead to higher levels of failure. White Paper 1 also showed that designing for HBM would guarantee adequate levels of intrinsic MM performance and that specifically testing for MM was not necessary. “White Paper 2: A Case for Lowering Component Level CDM ESD Specifications and Requirements” [2] made a similar case for CDM levels below 500 V by

presenting explanations of why high levels of CDM performance were not necessary and presented data to back up the arguments.

White Paper 1 (WP1) and White Paper 2 (WP2) were influential in changing the industry's mind about the level of ESD robustness needed to allow high yield manufacturing of systems. OEM's had a lingering concern however; what will lower component ESD levels do to system reliability? It has been assumed by many that the first step in producing ESD robust systems is to choose components with high HBM and CDM levels. The assumption that higher HBM and CDM levels will automatically produce ESD robust systems seems logical, but members of the Council knew this assumption was not true and that it was blocking the adoption of more reasonable HBM and CDM levels. The Council decided to address the problem with a third white paper to demonstrate the lack of correlation between component level ESD and system level ESD, and to address the wider question of how to effectively design for system level ESD robustness. Although *ad hoc* system level ESD designs have been done in practice, the important message of the White Paper 3 (WP3) Part I was to remove the misconceptions about system level ESD.

System level ESD is a very broad subject and differs substantially from HBM and CDM ESD. HBM and CDM tests only look for physical damage to unpowered ICs. System level ESD is most often performed on a powered and functioning system, and failures include not only physical failures but system upset. Due to the broad subject of system level ESD, WP3 has been divided into two parts. Part I focused on physical failures and the lack of correlation between component level ESD (HBM and CDM) and system level ESD. Part I also introduced the (basic) system-efficient ESD design (SEED) strategy for designing ESD robust systems. In this document, WP3 Part II, we address the broader topics of system level ESD design and system upset by an advanced SEED concept. For those not familiar with WP3 Part I a summary has been placed in Appendix D. The remainder of this chapter will preview the content of WP3 Part II.

We would also like to reference a recently published white paper by JEITA which addresses system level ESD related tests of ICs as used by the Japanese Industry [3]. Tests based on 200 pF/0 Ohm and 200 pF/100 Ohm RC discharge circuits are discussed to characterize transient latch-up robustness of powered ICs. The JEITA white paper focuses on this specific test procedure while this white paper discusses the general design approach.

1.1 White Paper 3 Part II: Summary of Chapters/Appendices

Chapter 2 looks at how ESD affects systems, beginning with how these events are coupled to internal system circuits and devices, followed by the system response (both hard and soft failures) and concluding with analysis methods used to determine root causes of upsets and failures. Included are methods of categorizing failures and coupling modes to internal circuits. Also described are classic trouble-shooting methods for solving ESD upset problems plus new technologies capable of identifying sensitive circuit areas and components.

Chapter 3 examines the advantages and limitations of ESD/EMI design methodologies as they are presently practiced. State-of-the-art ESD/EMI design methodologies span the continuum from comprehensive theoretical 3D modeling of Maxwell's equations for an entire system to the most basic trial and error bench tests, and numerous advanced practical and theoretical tricks-of-the-trade in between. Utilizing one or more of these methods in the concept, design, and prototype

phases, a designer can observe and improve the extent and effectiveness of any element or flow in a process intended to balance ESD/EMI robustness, system performance, and cost.

Chapter 4 summarizes the SEED approach. In the SEED approach the path of the ESD stress is analyzed and predictions of system response are made using the properties of the printed circuit board and components on the board. Not all ESD paths are the same, however. ESD stress can range from high energy stresses, which are directly coupled from a system IO connector to a sensitive pin on an integrated circuit causing physical damage, to a much lower energy stress that is capacitively coupled to sensitive circuit nodes and results in system upset, but no physical damage. This chapter categorizes the types of ESD stress which a circuit can be exposed to and shows how different approaches and circuit properties will be needed to analyze the different stresses and prevent system failures.

Chapter 5 describes the models and analytical tools needed to support the SEED concept. The first requirement is a standard model for the description of integrated circuit IOs. After describing the requirements for a standard model, existing models are examined that may be extended or adapted for SEED requirements. Next, simulation tools that use these models are also examined for their adaption to SEED. This is followed by an examination of the limitations of both software and hardware analytic tools. Finally, an example using available models and tools is presented.

Chapter 6 presents a summary of the white paper and final conclusions. The white paper shows that there are tools available, such as transmission line pulse (TLP), which can study component properties in the ESD time and current domain as well as scanning tools which can measure the propagation of ESD events through a system and locate sensitive circuit nodes. The white paper categorizes the paths through which ESD stress can enter a system and outlines how to analyze and design for these types of stress. To use this increased understanding, design tools need to be upgraded to handle the information from the extended characterization tools and to perform the analysis needed to quantify the behavior of the paths through which ESD stress enters a system. The models used to describe components need to be modified to extend their useful range into the current, voltage and time domain of ESD events. Finally, component manufacturers need to characterize their products outside the range of normal operation so that system level ESD design can be done based on known component properties. This can only be done with extensive dialog between system designers, measurement equipment manufacturers, electronic design automation (EDA) tool vendors, model file developers and component suppliers. However, this paper does define the important issues and provides a starting point and significant first steps in this dialog.

Appendix A addresses the typical stress conditions and design solutions used in various fields of electronic industry ranging from mobile phones, medical devices, computers, consumer electronics, and automotive components to avionics. It provides an overview of test standards to be applicable beyond IEC 61000-4-2 and discusses the impact of the multiple stress requirements on the design solutions. The applicability of the previously introduced SEED concept is analyzed for the various types of systems.

Appendix B addresses the changing technologies from different points of view that are slated to have an impact on the design capability of system level ESD protection. The main objective of this appendix is to review the integrated circuit technology roadmaps and trends with consideration to the system level ESD performance of information technology (IT), communications, and automotive electronics. The various issues that are critical for these trends

include IC package development into more complex 3-D structures, new advances in board assembly techniques, emerging optical interconnects as applied to IC connections, and the promising development of novel suppressive materials such as polymers with embedded nano-particles that can potentially offer low-capacitive and efficient solutions at both the package level and the board level. In its overall essence the appendix assesses the impact of rapidly advancing technologies on system level ESD requirements and designs. While not specifically recommending any future system level ESD specs, the appendix points to where the difficulties could arise from scaled down technologies, higher speed circuit designs, and broader analog and high voltage applications. The appendix also attempts to include some comments on the demands for resources and the cost for system ESD designs from the perspectives of both IC suppliers and system builders.

Appendix C describes how ESD threats to systems include both a fast component, from the ESD gun's initial current spike, followed by a slow component, with lower current but with considerably longer duration. The appendix explains how the current paths for the two components can be very different, can cause different types of failures and require different solutions. The section ends with diagnostic suggestions for locating susceptible areas within a system or circuit board.

References

[1] Industry Council on ESD Target Levels, "White Paper 1: A Case for Lowering Component Level HBM/MM ESD Specifications and Requirements," August 2007, at www.esda.org or JEDEC publication JEP155, "Recommended ESD Target Levels for HBM/MM Qualification", www.jedec.org

[2] Industry Council on ESD Target Levels. "White Paper 2: A Case for Lowering Component Level CDM ESD Specifications and Requirements," Revision 2, April 2010, at www.esda.org or JEDEC publication JEP157, "Recommended ESD-CDM Target Levels", www.jedec.org

[3] JEITA document EDR-4709, 2012

Chapter 2: Overview of ESD Stressing and System Response

Jon Barth, Barth Electronics
David Eppes, AMD
Leo G. Henry, ESD & TLP Consulting
Mike Hopkins, Amber Precision Instruments
Marty Johnson, Texas Instruments
David Pommerenke, Missouri University of Science & Technology

2.0 Introduction

The purpose of Chapter 2 is to look at ESD system level testing as it is done today as well as the complications (including coupling issues), failure modes, and trouble-shooting methods used to determine root cause of failures. "Soft" failures, where no obvious component damage occurs, and "hard" failures, where component damage *is* apparent, are discussed in some detail. Considerable attention is placed on electromagnetic coupling modes and the propagation of electrostatic discharges in a system. New evolving methods such as susceptibility scanning, software tools and system specific test boards to monitor the health of a system are all discussed.

2.1 Presently Used Stress Tests for ESD

There are presently only a few basic stress tests used in the industry for testing systems for the effects of electrostatic discharges. These are:

- **IEC 61000-4-2** and its derivatives for compliance testing of virtually all consumer, telecommunications, medical and light industrial electronics.
- **ISO 10605** for automotive electronics.
- **DO-160** for commercial avionics.
- **CDE (cable discharge event).** There are various corporate standards in use, and at this writing, Electrostatic Discharge Association (ESDA) is close to issuing a draft standard practice to help standardize test methods for CDE.

The following sections summarize these tests. For a more detailed discussion see Chapter 2 of White Paper 3 Part I [1].

2.1.1 IEC 61000-4-2

IEC 61000-4-2 applies a standard test methodology to equipment, systems, subsystems and peripherals that could be exposed to ESD events in the final installation. The environmental conditions (humidity, flooring materials, low-conductivity carpets, grounding methods) may influence the intensity of the discharge, which in turn affects the susceptibility to damage of the systems to an ESD event, and for the purposes of compliance testing, this standard closely defines the conditions under which testing is to be done. IEC 61000-4-2 specifies a current pulse that is quite different than those used for testing integrated circuits for ESD during assembly and packaging and is not correlative.

2.1.2 ISO 10605

ISO Standard 10605 is used to characterize the ESD sensitivity of electronic subsystems in road vehicles. This standard draws on the IEC 61000-4-2 for most of its procedures and physical set-ups, but adds three additional current impulse variants for conditions specific to the automotive environment. It applies to discharges in the following cases:

- ESD in assembly
- ESD caused by service staff
- ESD caused by occupants

ISO 10605 applies to all types of road vehicles regardless of the propulsion system (such as spark-ignition engine, diesel engine, electric motor) and for some cases requires testing to 25 kV.

2.1.3 DO-160 Section 25

This document is used to test airborne equipment (avionics) for the effects of static discharges from human contact. It is based on IEC 61000-4-2 and uses the same ESD test pulse. It consists of a 15 kV air discharge test applied to points on operating avionics that are accessible to people.

2.1.4 CDE Testing

This test is designed to determine the susceptibility of electronic products to electrostatic discharges that occur when a cable, such as Ethernet or universal serial bus (USB), are connected. If a charge differential exists between the cable and the product being connected, a discharge will occur to the affected IO pins. A proposed ESDA document provides test methods using both the ESD gun and a modified TLP system.

2.2 Definitions

2.2.1 Hard vs. Soft Failures in Systems

Both hard and soft failures in an electronic system can be induced by transient events from outside the system, such as noise transients on connecting cables and electrostatic discharges, but also by over-voltages due to mis-operation or improper connection of the system. In any case, the system has ceased to operate as intended.

A “hard” failure is one where the outside event has caused damage to a component that will require a service technician to replace the affected component. Examples of hard failures include damage to gate oxide, resistors and metallization in the signal path which could have been as a result of latch-up or overvoltage. These will all be discussed in more detail later in this chapter.

A “soft” failure is one where the outside event can have several effects. Using some definitions paraphrased from IEC documents, one can demonstrate these situations:

- System automatically recovers with no loss of data and no operator intervention. This upset is completely transparent to the operator. An example might be a change to a command or data stream that is caught and corrected by system software.

- System malfunctions in a way that the operator notices but operation continues. Examples might be interference to or momentary loss or distortion of a display, keystrokes that are temporarily corrupted or not recognized, or static or noise in an audio system.
- System malfunctions in a way that requires some recovery action be taken by the operator. Examples might be system lock-up, display becomes blank, controls or keyboard ceases to function. Typically, this kind of upset or malfunction requires powering down the system and re-booting.

In the above scenarios data could be corrupted or lost without being apparent to the operator. Under IEC definitions, loss of data is never allowed when testing a product.

2.2.2 Sub-Assemblies and Modules

The definition of a system is generally considered to be a completed, self-contained product such as a cell phone or lap top computer; however, for testing purposes, a system can also be a sub-assembly or module such as a video card, engine control module (in the automotive industry), or other device which can only function as part of a larger self-contained or distributed system. Sub-assemblies such as these (except automotive) are now included under the European Union's EMC Directive and must be tested as systems with similar failure criteria.

Testing and evaluation of sub-assemblies and modules present an obvious problem: the device being tested needs to be operating in a larger system to properly test for susceptibility. Ideally, it should be tested in the actual system where it will reside, but this isn't always possible. Take for example the manufacturers of sound cards, video cards, memory modules and other devices that could be assembled into a wide range of systems. These manufacturers may elect to test their product in a typical installation – a computer with known susceptibility characteristics – or in a test jig. It's up to the manufacturer to decide the best way to test the product to insure compliance, and often a system manufacturer, who is going to purchase and use the sub-assembly in question, may require testing in a specific way.

2.3 Coupling of ESD into Systems and Circuits

2.3.1 How Does ESD Couple into a System and Affect a Specific Component During System Level Testing?

Depending on the requirements of the test standard, system level tests typically require discharges to system enclosures and controls and may include some externally exposed pins. IEC simulators produce currents and transient fields and the resulting current pulses have been described as having both CDM and HBM like characteristics. Furthermore, they induce strong electromagnetic fields, which are not necessarily associated with the discharge current; including those fields that are also excited by the discharge relay used for contact mode testing (i.e., the ESD current is directly injected into the test object through metallic contact between the tester and the device under test (DUT), as opposed to an air discharge between the tester and DUT). Annex D of the IEC 61000-4-2 standard (2009) [2] provides good insight and further details the effect of different sensitivities and coupling mechanisms [3].

During discharges to system enclosures the injected current pulse spreads at close to the speed of light over the metallic surface of a metallic enclosure. This occurs because the current must

satisfy the tangential electric field boundary condition; Etan = 0. This can only be fulfilled by the creation of a current on the surface. At locations on the enclosure where the current has to divert due to the presence of slots or openings, fields will couple from the outside to the inside of the enclosure causing transient electromagnetic fields inside the enclosure ranging from very small to very large (kV/m). Furthermore, the current pulses will reflect on edges of the enclosure and couple to attached cables, predominately in common mode, which can then be converted to differential mode currents and possibly cause system upset.

The current densities flowing on the inside of the enclosure, its cables and PCBs are associated with strong electromagnetic fields. The electric fields can couple capacitively while the magnetic fields will induce voltages in any loop they can penetrate. The net effect of the dynamically changing electric/magnetic field strengths and localized field are induced voltages and currents. The induced voltages are often pulses of < 2 ns in width. Typical coupling scenarios are:

- A current flowing on the outside of a personal computer (PC) close to the peripheral component interconnect (PCI) slots of the enclosure will couple from the outside to the inside as the PCI slots are not well connected. Once the fields enter the inside, they can couple to any board, such as a graphics card, upsetting that board.

- The current from one PCB is coupled to another PCB connected by a flex circuit cable. The flex circuit cable does not confine the fields of the wanted signals well, and as a consequence the common mode current of the ESD on the flex cable can couple easily to signal traces.

- A current is injected into an audio trace, which is robust against ESD. This trace is routed inside the PCB parallel to a reset line. The coupling between the audio trace and the reset line causes noise pulses on the reset line; upsetting the system.

- A charged cable is plugged into a USB port. The ground contacts first and a large current is injected into the shell of the USB connector. This will cause a voltage drop between the USB connector shell and the chassis (as the connection is not perfect, but it forms a small inductance). The voltage between the shell and the chassis is visible on both the outside and the inside of the enclosure, and will force a current on the inside of the enclosure. Furthermore, although the shell connected first, a voltage is induced on the differential pair, which may upset a USB hub.

The fields can also interact with the direct current (DC) voltage supplies. While this is likely to lead to upsets if an IC's internal power nets receive large amounts of current from an ESD event, it is unlikely to upset power planes on circuit boards. The high decoupling capacitance and low impedance of typical board supply planes tend to limit the induced voltage, consequently, upset or damage is seldom seen by ESD injection to circuit board power planes. If power plane or ground plane injection causes ESD upsets, the mechanism is not the result of DC voltage fluctuations, but rather due to the transient fields of the ESD event coupling into other nets or directly into ICs.

For test standards requiring discharges directed at exposed pins (such as USB ports) or plugged in fixtures that simulate system events like cable discharge, the current pulse will travel from the connector to board traces which direct charge to the component pin. ESD injected into an input or output pin will typically be diverted to the internal positive voltage supply (VDD) and negative

voltage supply (VSS) net within the IC. However, the internal voltage transient can cause soft failures or hard damage. The effect of both signal and supply transients will be discussed in more depth later in the chapter.

Depending on board layout, trace length/thickness, signal shielding, and the passive/active components connected to a board trace or plane, the resultant reactance of the signal trace will attenuate rise time, duration and peak current as seen by the targeted IO or supply pins. This ultimately affects what happens to the charge when it gets into a system.

2.3.2 What Happens When the Charge Gets into the System?

The hybrid CDM and HBM characteristics of IEC simulator pulses results in high peak currents and pulse durations on the order of 60 ns at the point of charge injection. The degree of ESD pulse attenuation/degradation before arriving at the part will determine how the on die IO and power supply protection reacts. Attenuation of a pulse that would otherwise exceed the built-in protection capability could help protect a part from damage. However, if the perceived pulse characteristics fall outside of the component protection design window, the attenuation could also inhibit the response of pin level protection circuits as well as the resistor/capacitor (RC) triggered supply clamp. The net effect of inhibited ESD protection response could be failure at voltage levels lower than those seen by a component during component testing.

Signal attenuation can affect the way internal supply rail power clamps engage to dissipate the charge that is dumped onto the rail when the ESD diodes turn on. Power clamps often use triggers that expect a certain voltage rise time to engage. If clamps engage quickly and their current shunting capacity is not exceeded, the component should be protected. If the clamps turn on too slow or not at all, overvoltage damage of transistors connected to the supply rail can occur.

Because component protection is designed for an unpowered component, the response of a component when power is applied in a system and IO pins are transitioning can be much different. In some cases, the response can be inhibited because the ESD protection circuits see voltage on output pins and DC bias on internal supplies. These voltages affect the threshold at which protection schemes, like double diode [4], turn on and consequently the ability of the pin level protection circuits to shunt current. ESD power clamps that expect to see ESD pulses with the part unpowered now see pulses on top of a pre-existing DC bias. This voltage starting point, along with the possibility of a change in the time constant of an ESD pulse due to a reactance contribution from the voltage regulator, can retard the response of the power clamps.

The scenarios described above do not take into account external signal/power protection that may reside on the board to protect from system events. Transient voltage suppression (TVS) components protect a component by shunting charge before reaching the component. However if the TVS component does not fully shunt the signal, and the rise time of the residual IEC gun pulse is not fast enough to engage the on die supply clamps, overvoltage damage can occur as described above.

Coupling to signal or power lines adjacent to a targeted signal line can also lead to failure in signals or supplies that are not stressed directly. These lines may not have the same degree of protection as lines leading to the outside world. Failure of these lines will depend on the degree of coupling and protection on the coupled IO or supply.

2.3.3 Recoverable or "Soft" System Failure Modes

Many of the IO and power supply overvoltage/transient issues that cause hard failures at a given voltage may cause recoverable or soft failures at a much lower voltage, causing a system upset or a change of state in the system. Typically, the upset levels are much lower than the destruction levels. Signal or voltage supply rail (such as VDD or VSS) pulse induced transients is one mechanism that could lead to a loss of state of a system component, requiring user intervention to reset the system. Transient latch-up due to ESD pulse induced power glitches, or locally induced overvoltage of a power domain or cluster of transistors in a discharge path is another mechanism that could lead to a loss of state of a component/system.

2.3.4 System Degradation

In theory, so called "soft damage" to a transistor could lead to system performance degradation, which could be considered a system level failure if the degradation is self-detected by the system. An example would be soft oxide damage to an output driver transistor of a stressed pin which affected the robustness of the transistor. The driver could continue to operate satisfactorily at low frequencies, but higher frequencies or low supply voltage could lead to failure. Soft oxide damage due to voltage transients on voltage supply rails could also lead to degradation of internal circuit paths that ultimately affect performance as well. Passive components on system boards can also be damaged to the point that performance is degraded. Examples are surface mount chip capacitors and resistors used for filtering or terminations. Over voltage/current damage can change the effective value of these components to the point the circuits malfunction if they continue to degrade after initially being electrically damaged. This is sometimes referred to as a "latent" failure: one which occurs at a later time due to damage from a transient at an earlier time.

2.3.5 Hard System Level Failure Modes

Unlike a functional powered up system which can put a component in many states (and consequently induce many different types of failures), the state of a standalone component prior to the initiation of component testing is constant. System level testing can induce hard failures that would appear similar to those seen in component testing. There are extra failure modes that can occur in system testing that don't occur in component testing, but some of the more common component testing failure symptoms that could be seen in system level testing includes [5]:

a) Damage to gate oxide and/or channel damage to drivers and receivers attached to an IO signal.
b) Damage to primary signal path ESD protection circuits such as ESD diodes whose purpose is to protect the signal path. This occurs when the robustness of the protection circuit is exceeded.
c) Damage to resistors and metallization in the primary signal path.
d) Overvoltage damage to transistors which reside in power domain(s) and absorb charge routed to them by the ESD protection circuits. This occurs when the protection circuits (diodes, clamps, etc.) for the power domain fail to respond fast enough or their robustness is exceeded.
e) Latch-up

Because component protection is designed for an unpowered component, the response of a component when power is applied and IO pins are changing state is much different. In some cases, the response can be inhibited. This can be due to the following causes:

a) ESD protection circuits on IOs, such as protection diodes between the pin and internal VDD rails, are designed to shunt to unpowered rails. Voltage on the rail affects the effective voltage threshold of the protection diodes. For a diode with the anode connected to the pin and the cathode to VDD, the voltage threshold increases with bias. Elevated thresholds result in higher pin voltages during discharge, which typically increases the voltage seen by downstream circuits during a discharge.
b) dV/dt (for example, RC) triggered ESD overvoltage internal supply clamps that expect to see ESD pulses with the part in an unpowered condition now see pulses that start from a powered condition. This pre-existing voltage, along with the possibility of a change in the RC trigger time constant due to a reactance contribution from the voltage regulator, can retard the response of a clamp trigger circuit.

Aside from traditional component level ESD damage and damage due to inhibited ESD protection, localized voltage differentials which are not seen in standard operation could lead to latch-up of transistors. This can cause hard damage to a component if the latch-up condition is sustained. In theory, signal corruption due to an injected pulse could lead to a loss of state and signal "contention", where transistors are simultaneously driving opposing signals that lead to electrical overstress and permanent damage if sustained.

2.4 Troubleshooting to Determine the Cause of Failures

2.4.1 Hard Failures

Classic methods of troubleshooting electronic products work well in the case of hard failures. Faulty sub-systems, boards and finally components are systematically isolated by measurements of power supplies and signal tracing. In the case of hard failure of a component, damage is often detected with methods such as photon emission microscopy (such as emission microscopy (EMMI)) and/or laser induced circuit perturbation (such as thermally induced voltage alteration (TIVA)) that highlight circuit damage. These are well understood and documented techniques [6], and as such, won't be dealt with in this paper.

2.4.2 Soft Failures

Classic troubleshooting methods don't work well on soft failures simply because there is no physical evidence to find. Either the system recovered on its own through error correction routines or re-booting the system corrected the error. Soft failures are often found during compliance testing for ESD (as well during other types of immunity testing) but they also occur in field at the customers' site. In either case, the root cause of the failure needs to be determined and corrections made to the system to prevent further upsets.

When a soft failure is detected, the method of troubleshooting is often trial-and-error. This can be effective when the person doing the troubleshooting is familiar with the system, but if the failure occurs in the field or at an outside compliance lab that may not be the case. Even for a soft failure being investigated by someone familiar with the system architecture, the real root cause may still not be resolved although the symptom may be eliminated. Filtering, shielding or the addition of

protective components can be effective at removing the symptom, but the root cause might actually be a power bus running too close to a sensitive control line. Adding components may resolve the soft failure issue, but the real root cause -- the design problem -- remains un-detected.

One method of localizing a soft failure problem that is sometimes used is injection of a localized magnetic field or other disturbance in the vicinity of the suspect circuit. By moving the probe around the circuit and watching for upset it may be possible to determine the area of a board likely to be the problem. This method has recently been automated to allow very precise scanning and provide a 3-dimensional picture of a circuit board's weak spots and will be described in detail in the following section.

2.5 New Technologies for Determining Root Cause of Failures

2.5.1 Susceptibility Scanning

As discussed above, once a system fails due to a system level ESD event, isolating the root cause can follow different paths. For soft failures the most promising tool is local magnetic or electric field injection using susceptibility scanning. This can be performed by hand as previously mentioned but it is very difficult to obtain significant precision or generate a visual picture of the boards' sensitive locations. When done automatically [7, 8], these difficulties are removed and the ability to generate data for later analysis is achieved [9].

The objective of susceptibility scanning is to identify locations, ICs, modules and electrical nets that exhibit the same failure symptoms that were observed during system level testing. If those locations are found within the system, it is likely that during system level testing energy is being coupled from the outside to those locations, thereby causing the failure.

To identify these sensitive locations a locally strong field needs to be created that resembles the noise that might be coupled from the outside ESD generator to the suspect board or circuit. The methods are detailed in [7, 8]. In brief, a transmission line pulser having rise times of < 1 ns is connected to magnetic and/or electric field probes. These field probes are moved close to the ICs, nets or modules in question and pulses are applied by the TLP, which induces the field. The system reaction is observed. By varying the probe type, size and applied voltage, locally sensitive regions can be identified. Further, the results can be visualized as susceptibility sensitivity maps as shown below in Figures 3 & 4.

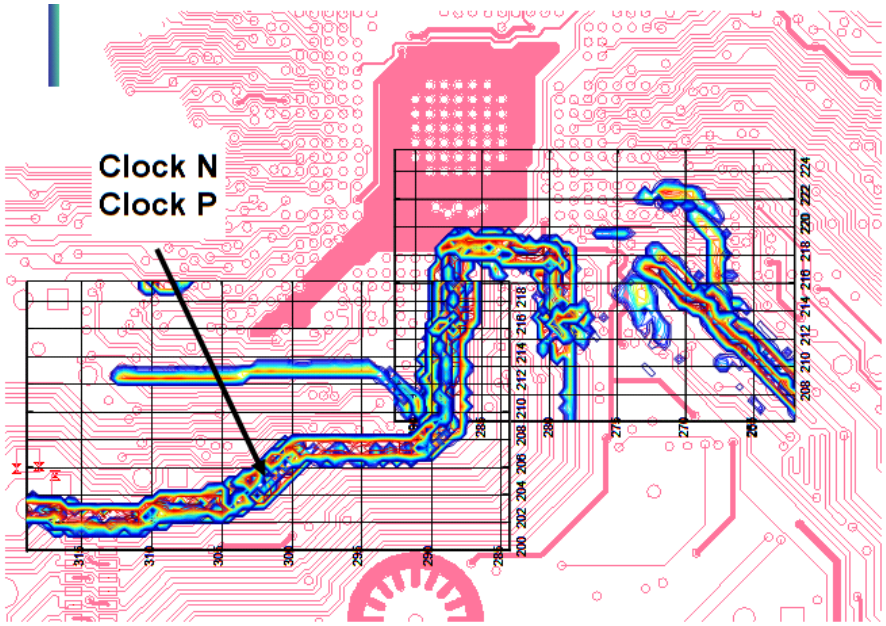


Figure 3: Result of susceptibility scanning: Sensitive differential clock on a motherboard [7]
(Courtesy of Amber Precision Instruments)

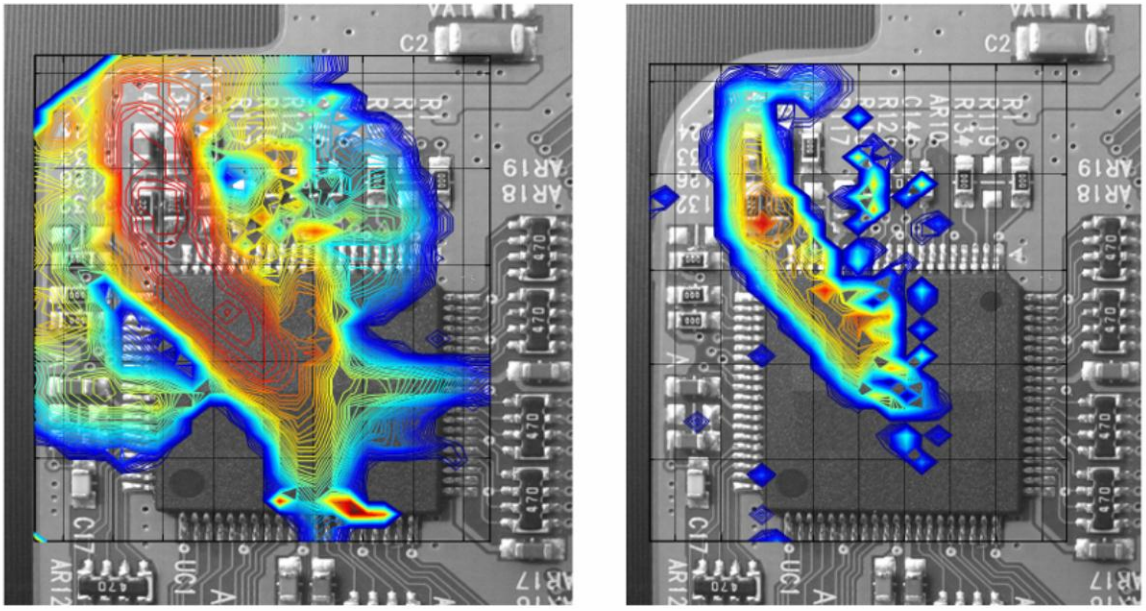


Figure 4: Result of susceptibility scanning: Comparison of two functional identical ICs from different vendors. The color grade indicates the TLP charge upset voltage with blue being 4 kV, red being 1 kV [7]
(Courtesy of Amber Precision Instruments)

2.5.2 New Software Methods

In addition to susceptibility scanning, software based methods can be used to uncover the root cause of ESD failures. These methods often require having pre-existing diagnostic tools built into the system that are targeted for debug. For system upset, where some system functionality is retained, software tools that collect the contents of die data registers can reveal status register bits, error codes, data loss or data corruption. All of this will provide insight into the nature of the failure. Other software tools include error handling routines that collect system response data for diagnosis but again, some system functionality must be retained to run the software diagnostic [10,11].

If system functionality is lost but components are accessible through special test modes such as JTAG (Joint Test Action Group) ports, it can provide another means of accessing the data registers. Factory debug and test modes can also be employed if they are available with appropriate documentation from the component manufacturer. Ultimately, for these tools to work, the system analyst needs to have a good working knowledge of the system and the information that can be extracted from the components.

2.5.3 System Specific Test Boards

System specific debug test boards are boards that can be embedded in a system to track and save system status for recall in the event of an ESD induced fault. Dedicated system monitor chips that report system status could also be used. Simple methods include fault indicator lights or display screen messages/codes that can point to unusual power consumption conditions by a component or else report the status of a component pin that only comes on during a specific fault condition.

When a failing component is identified and diagnostic information is gathered, component debug tools can be employed to isolate a particular location on a component. If the failing component can be exercised in the system to the point of demonstrating the mode of failure, various diagnostic tools can be employed including optical and infrared emission cameras and laser based scanning tools to pinpoint damage sites on silicon. Complications associated with use of these tools include special die preparation (die thinning) to support the optical nature of these tools. Software and/or system functionality may need to be modified to increase the acquisition rate of the optical signal. If the component cannot be operated in the system, it may be necessary to use special test hardware in conjunction with knowledge of the component to stimulate the failing condition. The complexity of the hardware can range from sophisticated automated test equipment (ATE) testers to curve tracers or DC power supplies.

Once a failure location is isolated, the next step is to understand the implications of the location of failure and, in some cases, the mechanisms seen in the physical analysis. Software based design tools that can correlate physical locations to circuit schematics are particularly useful for this analysis. The schematics can then be evaluated through analog circuit simulators such as simulation program with integrated circuit emphasis (SPICE) or digital simulators such as Verilog to confirm that the physical failure symptoms match both the analog response to ESD stimulus and the system behavioral response to the ESD upset.

As the response to a system failure becomes better understood, examination of physical die layout may be appropriate:

- If latch-up is suspected, the layout can be examined for latch-up design sensitivity.
- If damage to gate oxide is suspected, the circuit path that results in overvoltage during the stress event must be understood.
- If metal shorts or opens are discovered, the current carrying capacity of the metal routing at the affected location can be compared to the current expected during the system stress event.

2.6 Summary

It is important to recognize that both hard and soft failures occur as a result of ESD events in the test lab and in the field, and both need to be addressed. Component manufacturers rate components for their ability to withstand a certain voltage during handling, but an ESD event to a system producing only a few volts on an input pin of that component may cause a system to re-set unexpectedly. Fortunately, new software analysis methods and test instruments are becoming available to enable us to see what's happening as the result of an ESD event. This enables both the component and system manufactures to make good decisions in design that will save money and benefit everyone.

References

[1] Industry Council on ESD Target Levels, "White Paper 3 System Level ESD Part I: Common Misconceptions and Recommended Basic Approaches," December 2010, at www.esda.org or JEDEC publication JEP161, "System Level ESD Part I: Common Misconceptions and Recommended Basic Approaches", www.jedec.org

[2] IEC 61000-4-2, 'Electromagnetic compatibility (EMC) – Part 4-2: Testing and measurement techniques – Electrostatic discharge immunity test', Ed. 2.0, 2008.

[3] Jayong Koo; Qing C,ai; Kai Wang; Maas, J.; Takahashi, T.; Martwick, A.; Pommerenke, D., "Correlation Between EUT Failure Levels and ESD Generator Parameters", IEEE Trans. EMC. Vol.50, Issue 4, Nov. 2008 pp. 794 - 801

[4] Industry Council on ESD Target Levels. "White Paper 2: A Case for Lowering Component Level CDM ESD Specifications and Requirements," Revision 2, April 2010, at www.esda.org or JEDEC publication JEP157, "Recommended ESD-CDM Target Levels", www.jedec.org

[5] Anderson, W., Eppes, D, Beebe, S. "Metal and Silicon Burnout Failures from CDM ESD Testing", Proc. EOS/ES Symp., Sept. 2009, pp. 2A.6-1 - 2A.6-8.

[6] Voldman, Steven H., "ESD Failure Mechanisms and Models", John Wiley & Sons, Ltd, 2009, pp. 35-37.

[7] Muchaidze, G., Jayong Koo, Qing Cai, Tun Li, Lijun Han, Martwick, A., Kai Wang, Jin Min, Drewniak, J.L., Pommerenke, D., "Susceptibility Scanning as a Failure Analysis Tool for System-Level Electrostatic Discharge (ESD) Problems", IEEE Trans. EMC, May 2008, Vol 50, No. 2, pp. 268-276

[8] Kai Wang; Jayong Koo; Muchaidze, G.; Pommerenke, D.J. "ESD susceptibility characterization of an EUT by using 3D ESD scanning system", IEEE Int. Symp. on EMC, 8-12 Aug. 2005, pp. 350-355, Vol.2

[9] Zhen Li, David Pommerenke, "Electrostatic Discharge Induced Upset Probability Database for Transient Field Coupling to Integrated Circuits", presently under review (2012) IEEE Transactions on EMC, contact davidjp@mst.edu

[10] Maheshwari, P.; Tianqi Li; Jong-Sung Lee; Byong-Su Seol; Sedigh, S.; Pommerenke, D.; , "Software-Based Analysis of the Effects of Electrostatic Discharge on Embedded Systems", Computer Software and Applications Conference (COMPSAC), 2011 IEEE 35th Annual , pp. 436-441, July 2011

[11] Maheshwari, P.; Byong-Su Seol; Jong-Sung Lee; Jae-Deok Lim; Sedigh, S.; Pommerenke, D.; , "Software-Based Instrumentation for Localization of Faults Caused by Electrostatic Discharge," High-Assurance Systems Engineering (HASE), 2011 IEEE 13th International Symposium, pp.333-339, Nov. 2011

Chapter 3: State-of-the-Art ESD/EMI Co-design

Patrice Besse, Freescale Semiconductor
Jeff Dunnihoo, Pragma Design, Inc.
Masamitsu Honda, Impulse Physics Laboratory
David Pommerenke, Missouri University of Science & Technology
Pasi Tamminen, Nokia
Matti Uusimaki, Nokia

3.0 Introduction

The threat to a design posed by ESD is essentially defined by the term "Electrostatic Discharge," that is, the movement of an accumulated positive or negative static charge from the user environment to (or from) a component. The intensity of discharge that the component can withstand without damage or functional degradation defines its robustness and affects its cost.

Existing state-of-the-art ESD/EMI design methodologies span the continuum from advanced theoretical 3D modeling of Maxwell's equations for a system to the most basic trial and error tests, and all of the limited practical and theoretical implementations in between. A matrix of these approaches is presented in Table 1.

Table 1: Practical and theoretical co-design methodologies for ESD/EMI robustness

		Methodology Type	
		Practical	Theoretical
Complexity & Cost	Basic	Designer's experience, lessons learned, design reuse	Datasheet comparisons
	Advanced	Component qualification testing	SPICE modeling of ESD injection
	Comprehensive	Rigorous head-to-head system level iterative testing	Full 3D Maxwell Field-Solver Simulations

The overall design methodology is ultimately chosen to help the designer compromise on an optimum fixed point in the "tradeoff gamut" between three generally conflicting goals: (1) ESD/EMI robustness and susceptibility resistance, (2) signal integrity and functional performance (bandwidth, data-rate, minimum emissions, etc.), and (3) cost and/or time to market as depicted in Figure 5.

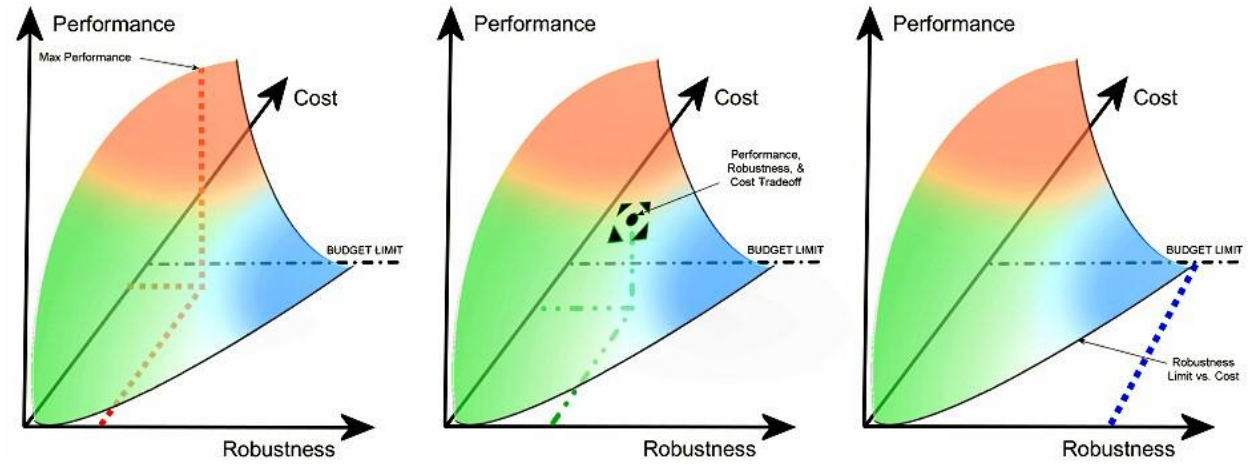


Figure 5: ESD/EMI Co-Design Tradeoff Gamut

This concurrent shepherding of sometimes cooperative but often conflicting design goals during product design and development is referred to here as the "ESD/EMI Co-Design" problem.

Not surprisingly, many of the protection strategies for ESD are tightly related to EMC robustness and EMI suppression methods. This chapter examines the advantages and limitations of existing and emerging methodologies in the art with respect to their effectiveness in arriving at the optimum robustness/performance/cost tradeoff for a given application. Obviously, the survey of such an extensive field is necessarily limited in its depth, but specific recommended system design guidelines are proposed.

From the beginning of the design process, critical exposed and susceptible nets must be identified and assigned reasonable and sufficient robustness levels, including the excess robustness protection margin desired. Aggressor pulse entry points or entry paths (whether conducted or induced) for hard and soft failures should be outlined as described in Chapter 2. Component selection, layout and placement should be considered with regard to ambient and direct ESD/EMI strikes and disturbances and the effect on signal integrity. System partitioning, grounding, clamping, shielding and return path shaping are also considered, along with the problems of potentially hidden multiple/secondary discharge points within the system.

By managing these issues in the concept, prototype, and design phases, a designer can observe and improve the extent and effectiveness of any element or flow in a process intended to balance ESD/EMI robustness, performance, and cost with existing and emerging methodologies. The remainder of this chapter will examine common examples of co-design as presently practiced, from the most basic rules of thumb, through advanced practical and theoretical methods, to comprehensive modeling of systems.

3.1 The Basics

As with any endeavor, a strong foundation or solid beginning can provide the most "Bang-for-the-Buck" in robustness vs. cost. Adherence to a few basic ESD/EMI principles and concepts throughout the functional design is often all that is needed to design an ESD robust system.

3.1.1 Shielding

The purpose of connecting a lightning rod and ground cable on a building is to route and shunt a potential lightning strike safely to ground in a reasonably controlled manner, away from flammable interior and structural components. Beyond encasing the building in a continuous Faraday Cage, the uncertainty and complexity of a strike makes the safe and cost-effective routing of the strike around delicate structures very difficult.

Consistent with ESD strikes on electronic systems, the primary goal for robustness design is to anticipate ESD entry points, and try to plan for effective return paths away from sensitive components.

While managing these primary effects, the designer also must be aware of potential indirect secondary effects of strikes or zaps, such as transient latch-up, or secondary discharges as described in Chapter 4.

The first and generally most effective method of protection is to encapsulate the entire system in a conductive enclosure, but as system input and output ports often do not permit complete enclosure, it will be necessary to add some holes in the enclosure for buttons, displays and connectors. These holes then become potential entry points for system level ESD strikes.

When these entry points are identified on or near susceptible nets (whether directly injected or indirectly coupled as discussed in Chapter 2), then discrete and/or on-chip protection circuits are often used in an attempt to catch and shunt ESD energy from the circuit back into the shield, and these methods are discussed in more detail below.

Good implementation choices made about how and where to implement limited shielding often provide the first and only protection needed for a sufficiently ESD-robust system. For example, certain systems naturally are constrained to certain standard IO connector requirements. A television (TV) or a monitor may require a high definition multimedia interface (HDMI) or digital visual interface (DVI) input. But whereas the bare HDMI connector presents tightly packed IO pins with interleaved ground pins and an enclosed ground shield as shown in Figure 6, the 0.100" (2.54 mm) pitch of the DVI pins exposes sensitive IO lines to potential unprotected strikes.

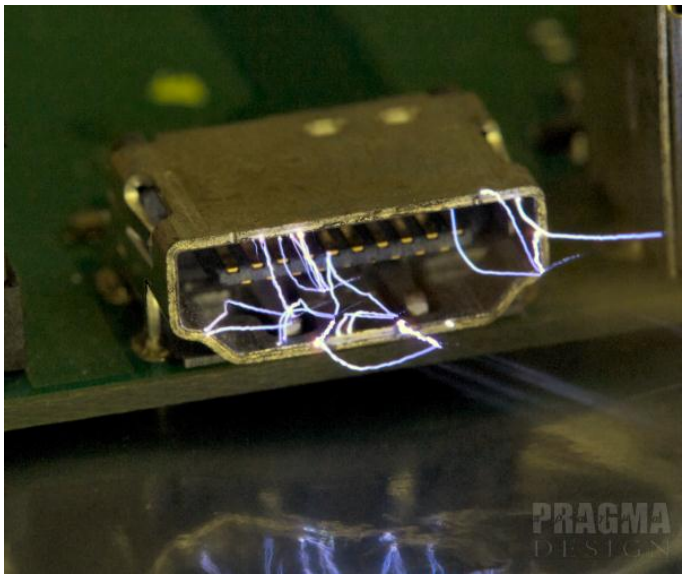


Figure 6: Multiple air-gap strikes to shield and pins as an entry point or aperture

A system is as vulnerable as the first component to fail during an ESD strike. But the mere selection of an interface type may also introduce some engineered "ESD robustness" embedded in the basic design of the interface (such as the connector grounding design mentioned above). Thus basic knowledge of typical IO susceptibilities may provide a large portion of the solution.

3.1.2 Beyond Shielding

Signals into and out of a system must be designed to handle the potential of unwanted ESD entry through those points. Once such a potential is identified, the design engineer must provide a preferential path to dissipate the strike(s). The following are the basic points to consider from the ESD perspective:

- Good Return: Provide good ESD ground return paths for connector shells and grounds, and TVS or other ESD attenuation components.
- Short Path: Clamp and divert ESD charge as close to the entry point as possible. Place TVS components or other attenuators as close to the entry point as possible to limit the total loop area and direct coupling of the aggressor pulse into safe paths.
- Hidden Impediments: Minimize secondary parasitics in the return path (for connectors, grounds, and clamping components). Consider component package parasitics and PCB plating/stackup considerations which may affect overall system parasitics.

For a more detailed conceptual analysis of guiding ESD current from the entry point out of the system, see Appendix C.

3.1.3 Component Selection

Any given system board will be populated with components of varying individual ESD robustness and protection. The same set of components implemented in different ways on the board, or within the system, may result in different levels of system ESD robustness.

While system specifications such as IEC 61000-4-2 are often applied to component evaluation boards as the "System-Under-Test," the results of these tests cannot be directly compared to system level testing of complete, end-user ready systems. Component suppliers are limited in their ability to accurately characterize the system level robustness of their particular component since the choice of other interconnected components, connectors, routing and enclosures is out of their control and up to the system designer. Even if a component supplier provides a "reference design" circuit with a particularly well-characterized TVS component combination, a poorly designed enclosure can dramatically affect overall system robustness.

For example, consider an ESD stress to an IO pin of an integrated circuit. If the IO is intended to be connected directly to a system IO, such as a USB or HDMI pin, it would seem that stressing the component's IO pin versus the component's ground pin would correlate directly to the IO pin's ESD performance in a system. The current path for a component ESD test may, however, be totally different from the current path during a system level ESD test. In a component ESD test, such as HBM, one pin combination (other pin combinations would look at IO to power rail or other IO) tests between the IO and ground, all current entering the IO pin must exit from the ground pin(s). In a system ESD test the current may all enter into the IO pin but the return path to the ESD source may include one or more power pins and have very little current exiting the integrated circuit through the ground pin(s).

Selection of components and optimal layout for the system may be the only degrees of freedom that a board or subsystem designer may reasonably have at his disposal. Determining component robustness from manufacturer specifications is not always straightforward. For example, consider the two TVS clamping components below in Table 2:

Table 2: Sample attempt at comparing and contrasting two TVS datasheets

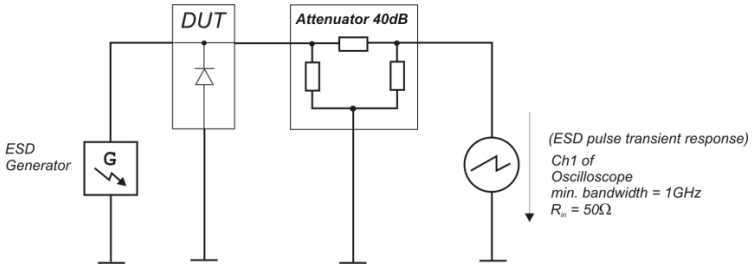
	Component A	Component B
ESD "Rating"	10 kV ???	8 kV IEC 61000-4-2
R_{DYN}	0.8-1.2 Ohms *IEC 61000-4-5 (8/20us)	0.6-0.7 Ohms *TLP 100ns
V_{CLAMP}	18 V *IEC 61000-4-5	240 V peak ???
Strikes	10 kV - 10 positive / 10 negative 12 kV - 1 positive / 1 negative	8 kV - 1000 positive / 1000 negative

The 10 kV ESD withstand rating of the TVS protection component "A" on its evaluation board initially appears better than "B's" 8 kV except that the test condition is not clear. But in any event, this only attempts to describe what the TVS component will withstand on its own, and tells nothing in particular about how well it can protect other components (For more information on the difficulties associated with testing components individually at the system level see Section 2.2.2 of Chapter 2 of White Paper 3, Part I [1], and Section B.7 in the Appendix of this paper).

The dynamic resistance is interesting in that it suggests that Component B might shunt more current from a node under protection than Component A, but upon further inspection we may find that the dynamic resistances are specified for different test conditions, test pulses, and stress levels. In the third row of Table 2, the "clamping voltage" is provided, although with a very low surge current (slow risetime, low bandwidth) in one, and a very high peak transient (fast risetime, high bandwidth) measurement setup in the other. In the end, the designer is left with essentially no meaningful comparison or contrast between the two sets of seemingly similar TVS parameters.

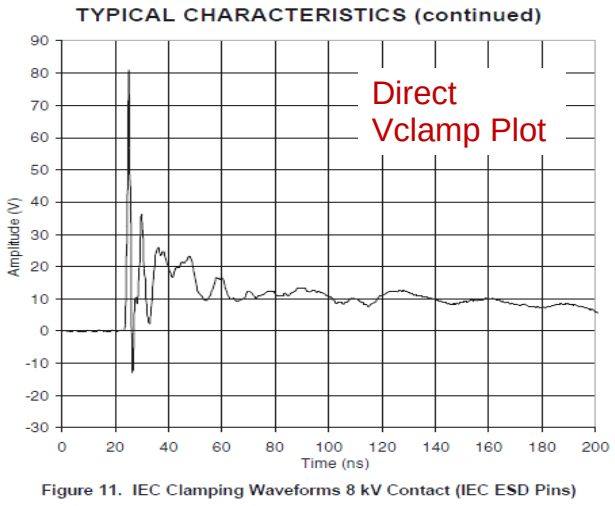
The last line of Table 2 reflects the attempts of some vendors to characterize the robustness with repeated strikes at a particular or multiple rated levels. These may imply a guarantee of survivability, in that either their component specifications will not change after repeated strikes, or that while the physical characteristics of the component may change dramatically within limits after repeated strikes, the absolute limits of the component specification will not be violated. While there is a maturing body of literature on repetitive damage in semiconductor and polymer clamp components, there presently is no accepted industry standard for the characterization or definition of "multi-strike" robustness or margin [2].

Even when components from the same vendor are considered under the same test conditions, the specification data may not provide meaningful comparative data for proper selection, especially when protection components are interacting with other components competing for ESD currents in a net and the sharing (and real-time behavior) becomes much more complex; see Figures 7a and 7b for typical examples.



Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{CL(ch)trt(pos)}$	positive transient channel clamping voltage	V_{ESD} = 8 kV per IEC 61000-4-2; voltage 30 ns after trigger	[1] -	8	-	V

Figure 7a: Example of a well specified ESD test condition, but with arbitrary test parameter reported.


TYPICAL CHARACTERISTICS (continued)
Direct Vclamp Plot
Amplitude (V)
Time (ns)
Figure 11. IEC Clamping Waveforms 8 kV Contact (IEC ESD Pins)

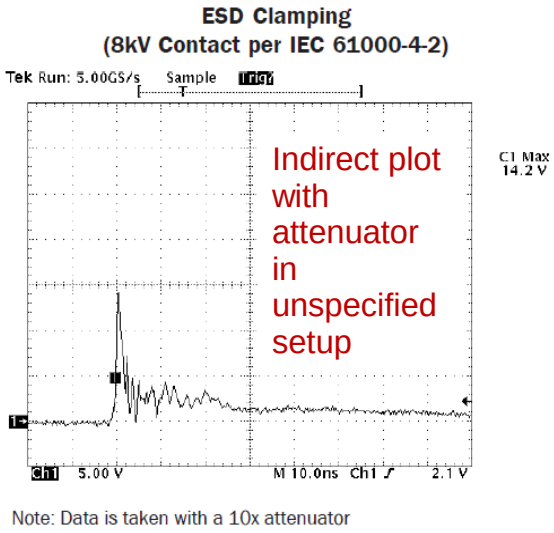
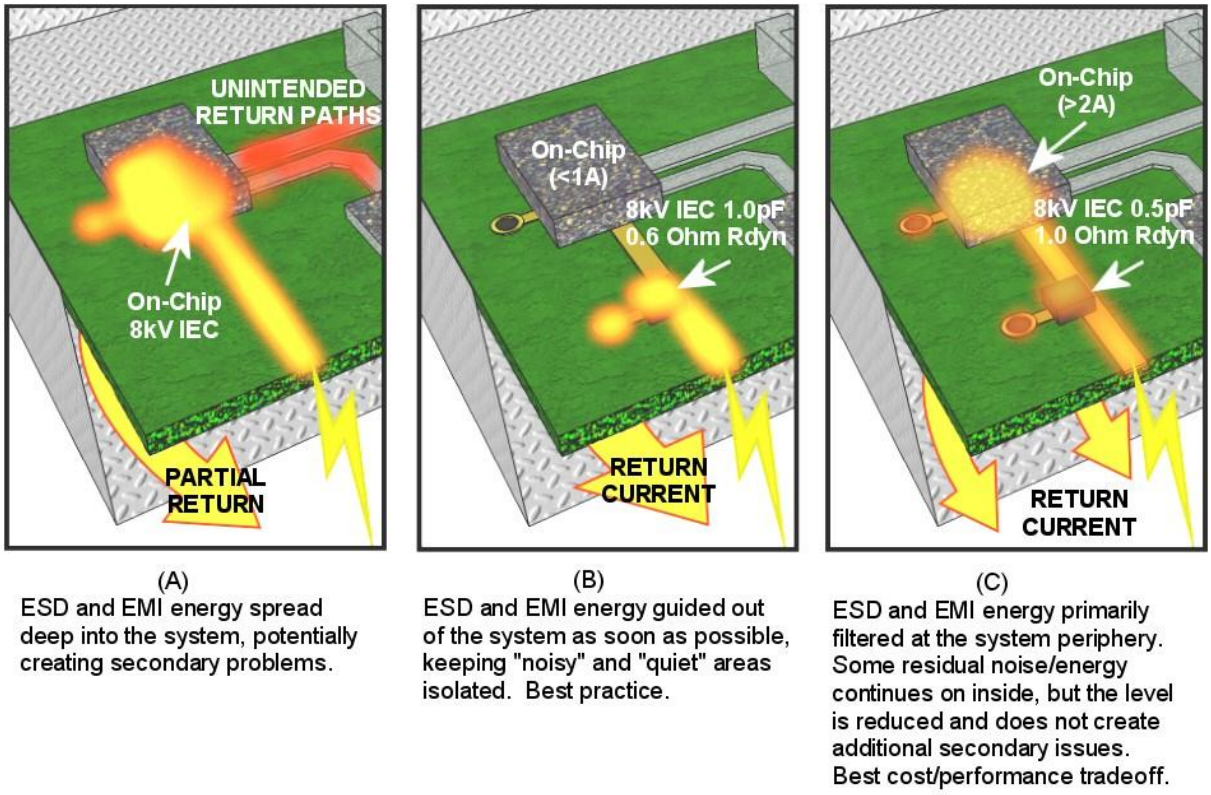

ESD Clamping
(8kV Contact per IEC 61000-4-2)
Tek Run: 5.00GS/s Sample
Indirect plot with attenuator in unspecified setup
C1 Max 14.2 V
Ch1 5.00 V
M 10.0ns Ch1 ƒ 2.1 V
Note: Data is taken with a 10x attenuator

Figure 7b: Competing examples of unspecified ESD test conditions providing peak clamping values also affected by unreported measurement bandwidth and test conditions

The result is that design reuse becomes an important safety line for designers from one product generation to another in the realistic climate of incomplete ESD comparison data available to designers today. Lessons learned about replacing Component A with Component B may encourage the designer to stick with a known design, and render him less willing to consider a cost reduction of New-and-Improved Component C. Without a reliable methodology to qualify the performance in-house in specific systems, the designer may be forced to forgo an otherwise margin-improving cost reduction.

3.1.4 ESD/EMI Budget Strategy

For critical IO nets, such as high-speed serial interfaces or radio frequency (RF) antenna connections, the system designer may be faced with a passive parasitic budget as well as a bill of materials (BOM) pricing budget. As illustrated in Figure 8, similar challenges exist for EMI filter design and TVS clamp selection where there is a direct external interface with signal integrity restrictions on filter and protection components.



(A)
ESD and EMI energy spread deep into the system, potentially creating secondary problems.

(B)
ESD and EMI energy guided out of the system as soon as possible, keeping "noisy" and "quiet" areas isolated. Best practice.

(C)
ESD and EMI energy primarily filtered at the system periphery. Some residual noise/energy continues on inside, but the level is reduced and does not create additional secondary issues. Best cost/performance tradeoff.

Figure 8: A qualitative illustration of RF ESD design issues with respect to ESD/EMI budget

In very critical design cases, minimizing the "ESD shunt budget" for each component may become a consideration as a way to attain a more desirable position on the Robustness/Performance/Cost tradeoff gamut. Since parasitic capacitance tends to increase with increased robustness in a TVS, a "weaker" TVS component may be chosen to obtain a lower parasitic capacitance that fits within the signal integrity design constraints. In order to maintain equivalent system robustness levels with the weaker TVS component, the component under protection will be required to shunt more of the "ESD shunt budget", otherwise the achievable overall robustness will be reduced.

For instance, a high-speed serial bus may allow for as little as 1 pF of additional parasitic capacitance on each IO line to pass compliance tests. If that port may be subjected to an 8 kV IEC contact strike, but the physical layer interface (PHY) chip can only tolerate a 2 A peak residual current, then there likely must be some additional external protection added to meet the system level robustness goal. Rather than choose an 8 kV, 1 pF, 0.6 Ohm TVS component that can

attenuate the majority of the system level pulse, the system designer may need to choose an 8 kV, 0.5 pF, 1.0 Ohm component that stresses the application specific integrated circuit (ASIC) closer to its maximum limits (Note again, as in Table 2, that while both TVS components might be "rated" at 8 kV, their effect on overall robustness and signal integrity in the system may be radically different due to their dynamic clamping resistance (Rdyn) and other parameters).

In this manner the "ESD shunt budget" is shared more efficiently between the two components (see Figure 8C). It is important to understand that this very critically allocated ESD budget should be contemplated in the most restricted circumstances. If the ESD pulse penetrates deep into the system (See Figure 8A) then secondary upset effects are more likely, meaning that there could be a secondary spark inside the system or at least the ESD return current on the ground plane that will generate additional noise effects.

This is analogous to a total distributed insertion loss budget for an inline EMI filter, where two filter components in series both contribute to the total budget. While the two filters could share the attenuation equally or in any arbitrary fraction, the majority of the EMI attenuation should occur in the elements closest to the connector to avoid "polluting" the interior of the system with interference.

Likewise, the ESD protection should be implemented as in Figure 8B, where TVS and filters are placed as close to the IO port as possible and the ESD is returned out of the board as soon as possible.

Both the EMI and ESD budgets are thus optimized by minimizing the overall design margins for the system. This potentially makes the system more vulnerable to both EMI and ESD; therefore this method should be utilized in only the most critical situations.

3.1.5 Equipment Ground

The ESD charge must be stored or returned in a manner that does not affect the operation of the system. This aggressor charge may be safely conducted along the perimeter of a metal product case to an alternating current (AC) mains ground line, or it may charge the volume between a laptop and a tabletop as shown in Figure 9. But it may also charge an IO input gate capacitance beyond its breakdown voltage, or it may be transformed into enough heat by an ESD clamp to permanently damage it.

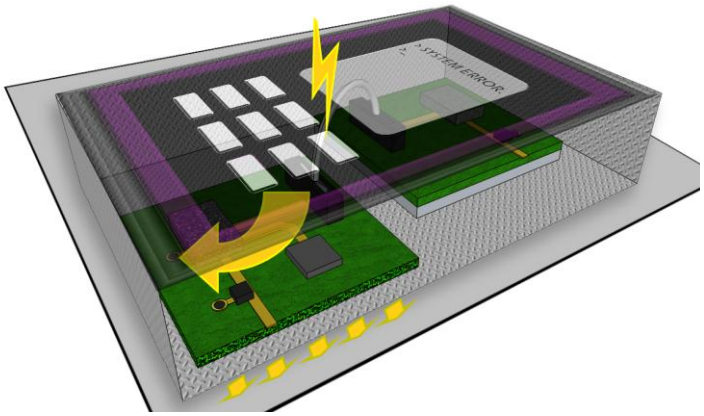


Figure 9: Discharge path into a keypad, through the system to a local ground, then through the case on the system return path (of a generic device as shown here)

Again, the overall ability to gracefully transfer or transform ESD charge without damage or functional degradation depends on a good system level path from the system to the outside world. What must be considered are the discharge paths from the system entrance point, to the different local ground nodes, to the PCB ground, to the case ground and to the reference ground of the system level test.

3.1.6 Quick Fixes

Even the best trouble-free legacy designs may suddenly exhibit an unexpected susceptibility out of the designer's control due to user application environment changes, unavoidable supply chain substitutions, end-of-life component revisions, or component variation interactions not anticipated during system design.

In this case, the immediate engineering problems for the designer are to "fix-what-we-have", and fix it fast! Unfortunately, this problem is resolved through the same design-for-robustness exercise applied during normal product development and design, except that the designer is now constrained to the existing board and components already committed to the supply chain. In this case, an "add-on" component may be the only hope to avoid complete redesign of the system board, if not the entire system. Again, the more information the designer has on failure and suspected "upset vector," the more accurately he can focus his solution options.

Some options include:

1. Enhancing shielding/grounding with copper tape or improved bonding of conductors, fasteners, product covers, cases and gaskets or other components.
2. Populating "depop" TVS footprints with additional clamping components if the pads were included initially as an insurance policy.
3. Upgrading the components to more robust (potentially more expensive) versions in the same footprint
4. Software recovery methods (catching and correcting ESD upset vectors, see Section 3.2.8)
5. Absolute last resort: Reduce qualification ESD level. (Often not possible for a given application.)

3.1.7 Information Available to the Designer

As described above, little helpful system ESD protection information is provided by component suppliers. System designers may consider external shielding as a first step. While placing a roll of copper tape on top of a laptop is not going to degrade the system ESD robustness, it is the skillful application of such tape/shielding, in the right amount and location, which can actually improve the robustness. Likewise, reactively adding TVS clamps on an IO may not help with the problem at all, and ironically may even make some system ESD problems worse.

System test qualification standards are universally accepted (and required for regulatory purposes, see Appendix A for examples) for various applications. However, as shown in Table 2 previously, a uniform test and measurement reporting regimen is not commonly adhered to by component vendors for *components* that comprise those systems.

3.2 Advanced System ESD Protection Methods

3.2.1 Primary Goals of ESD/EMI Co-design Today

The goal of ESD/EMI co-design in its present form is to primarily meet minimum ESD and EMI susceptibility and robustness qualification levels without affecting either the cost or the performance of the end product. Indeed, while best practice recommends extensive in-depth prediction and analysis of ESD performance, in reality many engineering groups include ESD as

part of a hit-or-miss qualification result. In all fairness, the complexity of this analysis, and the lack of accurate, inexpensive system level tools to do this analysis makes it almost impossible to justify more than a cursory basic approach to ESD robustness design for some low-cost, quick-to-market products.

Regardless of the pre- and post-design attention paid to ESD robustness, three key elements are considered in the "tradeoff gamut."

1) Sufficient Signal Integrity and Functionality
2) Adequate ESD/EMI Robustness and Compliance
3) Cost and Time to Market

3.2.1.1 Sufficient Signal Integrity and Functionality

The requirement for IEC 61000-4-2 based testing is to test it on a functional system. If the system is not functional to begin with, then IEC testing has no meaning.

Extending the extremely trivial example from the beginning of the chapter, if it becomes necessary to seal off all IO ports with copper tape in order to pass IEC testing, then your system results aren't meaningful. However, adding robust, high parasitic-capacitance clamps and/or series resistance to IO lines which limits the bandwidth or signal levels below the required performance is effectively the same as deleting the port from the system altogether.

Thus meeting the new performance and functional specifications are the first priorities in any design.

3.2.1.2 Adequate ESD/EMI Robustness and Compliance

EMI compatibility is not the primary focus of this paper, but it certainly overlaps the scope, as ESD immunity in many instances reflects a reduction in susceptibility of electromagnetic interference from electrostatic discharge. Very often, solutions for attenuating EMI interference (received or emitted) also result in signal attenuation at ESD frequencies.

The appropriate target for system level ESD is often set by the industry for a given class of applications through a plenary or composite standard (See Appendix A for examples). Sometimes, a corporate system ESD level is mandated for competitive or historical issues [3].

3.2.1.3 Cost and Time to Market

Less ESD protection cost usually means higher profit margins. Over-engineering the system ESD may be fine if it adds little to the total costs. Of course this is true for all costs and time, not just the product BOM. The engineering analysis cost for modeling, simulations and human resources for best-performance with optimum robustness may be much more expensive than simply relying on a known, slightly more expensive component.

Time to Market is directly and indirectly related to cost and sales/profit. One year of ESD simulation and co-design for a system on a 6 month design cycle to product release is unacceptable. Reducing expectations or missing product launches can impact entire corporate product perception or product reputations. So additional BOM costs and committed ESD development time must always be considered against schedule slips and field quality levels.

3.2.2 Desired Results vs. Actual Process Reality

State of the art ESD system design often relies on a core competence individual (or team) who can quickly analyze and recognize both ESD problems on a schematic or layout and also recover from the disaster quickly with "first aid" in the lab. The most effective tool in this kit is an understanding of ESD events, ESD damage, and ESD mitigation strategies and structures. This specialist may have responsibility on the design team, or may be a full-time ESD/EMI engineer in the corner office, or he/she may be found at a component vendor that can help spot the system problem or avert potential problems.

A further reality is that testing resources and equipment may not always be as readily available to the designer as a debugger or design consultant. These testing resources may not even be resident within the company but could be limited to an external test house. These testing resources may also be at a vendor or even integrated into a customer acceptance team. In this case, it is even more important for the designer and the ESD expert to communicate effectively with industry accepted and well defined ESD fault analysis and recovery concepts.

Examples of specific ESD-induced problems without obvious origination points include:

- Indirect test modes triggered by ESD noise superimposed on signals, op-code corruption due to glitched prefetched instructions.
- Air discharge induced into the case, PCB grounding and return path ground-bouncing, leading to in-band susceptibility issues.
- Direct injection into keypad IOs or USB thumb drive case through plastic enclosure seams.
- System component EOS failure where the root cause analysis from manufacturing line is determined to be the result of ESD-induced latch-up failure.

Each of these examples represents the end of a root cause analysis phase of investigation and the beginning of a transition to remedial design revisions to prevent the problem.

Any combination of these potential problems may have been lurking near the "robustness margin" surface and became a failure by chance, despite the best efforts of an ESD/EMI co-design methodology. But at the point of emergence, these problems must be identified and assigned to the appropriate resolution team. This team must not only identify the missed energy enclosure opening, but also the failure mechanism and hopefully remedial options, even if they cannot be immediately implemented.

This can result in a point of recovery, or a decisive breakdown in the development success. Pushing back on a component vendor or the manufacturing department, or even on operator error, may be justified in some cases. Either the failure criteria are too severe, or the robustness is insufficient for the application and the system designer must decide to either improve the product or relax the specifications. On the other hand, the design constraints may very well be such that there is no acceptable solution for a given target and the yield loss or product vulnerability must be tolerated.

3.2.3 Design Reuse

Reusing layouts and known components can help propagate the techniques and lessons learned in previous designs, or even result in accidental success. Conversely, changing everything from design to design won't necessarily make the design more or less robust, but reduces the confidence level that performance observed in previous systems is relevant to the new design. A different system layout, or the same system layout with a new revision of silicon, may provide radically different ESD results.

3.2.4 Revision Decisions

New revisions of silicon can unexpectedly impact the robustness of the system, even when all the specifications appear to be "improved." For example, an improved, faster clamping on-chip ESD protection circuit in an IO for an ASIC may trigger before an old reliable external TVS component and actually fail sooner than the TVS component when combined in the system.

Changes in silicon are obviously inevitable and usually desirable from both the cost and performance side of the "tradeoff gamut," and they often offer improvements in the robustness corner as well. But each deviation from a previous design correspondingly reduces confidence that the new design will (a) provide a similar level of robustness and (b) be responsive to tweaks and enhancements in the same fashion as the previous design.

3.2.5 Post-Design Iterative Improvement

After the new design prototypes are received, the moment of truth for any design is the test and validation phase of the predictions and simulations of the design phase. Obviously, the *cost margins* for the given BOM are easily calculated and well understood, and the *functional performance margins* of the system can be tested, but the third vertex on the tradeoff gamut, *ESD robustness* ***margin*** must also be assessed.

IEC system level testing helps ensure that a given sample system can survive a given strike level such as 4 kV contact (Level 2). But while one can measure bit error rates or eye-diagram margin on data links, IEC testing is pass/fail, and does not provide a statistical margin assessment of the robustness.

3.2.6 Robustness Margin Fine Tuning

Unfortunately, there is not a well-defined definition for the ESD robustness margin, much less an industry consensus for how to measure it. In general, it is thought that if a system passes 6 kV, then it could be said that it has 2 kV of margin above a 4 kV target. This is not as strictly informative or meaningful as it may seem.

For example, this borderline system may very well pass 4 kV once, but then fail at 4 kV if retested due to multiple factors; including number of strikes (variation in cumulative damage) or test/gun variability. The same system can vary by as much as 2 kV or more due to these issues [4].

Some vendors specify robustness beyond the defined standard test method to guarantee their component for multiple or even thousands of repetitive strikes. The intent is to provide a confidence level that cumulative damage (due to silicon filament formation for example) will not threaten the component performance with a fraction of the number of rated multiple strikes.

Additionally, the BOM may have many qualified supplier and version options for the same footprints, and these may impact the final cost substantially. So in addition to validating the absolute system robustness level for a given BOM selection and price, it is also helpful to quantify the relative robustness margin improvement for cost increments of different component choices.

3.2.7 Head to Head Component Comparisons

For example, if a board has a TVS footprint that will support two or more components with varying specifications, which component gives better ESD results for the price? If a system passes 4 kV with a 3 cent TVS part and a 1 cent TVS part in the same socket, then is the 1 cent part always a better choice? Alternately, if the system passes 6 kV with the 3 cent part and only passes 4 kV with the 1 cent part, is the extra cost worthwhile?

Building and evaluating a statistically significant number of systems each with different TVS components is usually cost prohibitive and impossible due to resource and time constraints, so often, this problem cannot be easily resolved.

One way that this is addressed is with low level head-to-head testing (same system with the only change being different TVS products) as described above. Additionally, testing from individual components (often supplied by the vendor under favorable conditions) is compared to results from other vendors. None of these methods are exhaustive, but can often identify an improved component selection option that can still meet the budget. This then becomes a hard-won starting point for the next design.

Sometimes the most critical comparison and contrast cannot be made under identical test conditions. For example, a typical Shunt TVS component may need to be contrasted with an improved Series-Shunt protection component as shown in Figure 10. Obviously, the 3-pin device cannot be directly tested on a system board designed for a 2-pin TVS device.

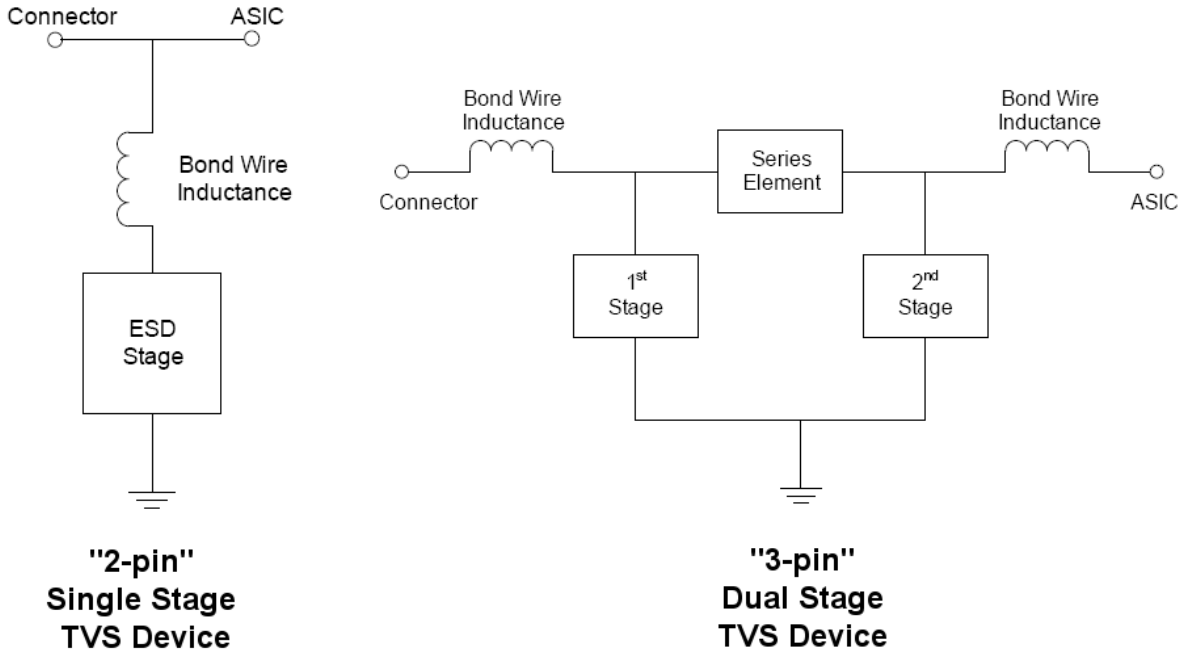


Figure 10: 2-pin "Shunt" vs. 3-pin "Series Shunt" TVS Clamps

The introduction of an alternative test board revision provides a concrete "what if" platform to evaluate. However, since the PCB must change slightly for different pinouts, the results cannot be assumed to indicate a strict accordance with the component's parameters only. PCB layout choices (such as vias, routings) will play a part in the end result and must be considered as well.

To extend this methodology to a quantitative improvement analysis, various methodologies described in Chapter 5 are being used to directly measure the in-system performance of components during actual ESD strikes. This comprises multiple samples of either complete systems or sub-assemblies being scanned during the strike, and then evaluating the evident current paths and levels. This is a very resource intensive exercise but may immediately pinpoint unexpected anomalies, which of course is the domain of ESD strikes.

3.2.8 Software Recovery Methods

In the case of readily repeatable soft failures and upsets, another remedy available to the system designer may be software or firmware patches and routines which can detect and correct the ESD upset condition. Normally, a digital system must assume that it is coherent, and that registers and state machines will not randomly lose their mind. But when ESD/EMC immunity is considered during a system upset, an external effect can invalidate many of the assumptions software may make about the rational machine on which it is running.

This is an immense subject area, which may be as complex as the software architecture of the system or as simple as a configuration bit setting. Additionally, this option may be severely limited by a lack of control over the software for the system. If an original design manufacturer (ODM) supplies an industry standard hardware platform intended to support multiple software stacks, software recovery methods may be impractical.

Consider the case where a codec is upset by ESD and merely loses its data link. An existing error correction algorithm may already remedy the ESD induced error as if it were any other signal integrity issue or "bit error" contemplated in the design. On the other hand, if the same functional block locks up but is not damaged and the rest of the system is stable, it may be possible for the driver software to recognize the upset state and seamlessly reset and reconfigure the block for operation, making the system operation appear uninterrupted at the user level. In such cases, a few lines of code may mean the difference between a pass or fail during ESD qualification.

In other cases, where the entire system resets, it may be necessary to add a discovery algorithm during the soft reset boot code that is able to recognize the difference between a normal warm boot and an asynchronous, ESD induced soft reset or upset. There is no set method to implement this mechanism, but often registers which are known to be upset to a certain state can give clues to the boot monitor as to what may have just happened and what recovery actions may be necessary. Watchdog timers and periodic interrupts, as well as dedicated system monitor microcontrollers which are already used in the system, may be adapted to help with ESD event recovery tasks. Below are some examples of "best practices" for software recovery or software robustness techniques in ESD/EMC co-design:

1. In low level configuration software or firmware, make sure that all unused IO ports are set as outputs, not inputs. This will reduce the possibility that floating inputs will accidentally collect some unexpected status inside the register. In the initial design, it may not cause any harm, but may impact subsequent software versions which may read that register or bit, making it difficult to analyse ESD susceptibility later on in the field.

2. For edge triggered interrupts that initiate critical functions, such a shutdown operation, it is a good practice to have a secondary check for the line before executing the operation. This would be analogous to the operation of a soft-power button debounce circuit. The action is edge-triggered, but the state of the button is validated only after the debounce period where the "ringing" of the mechanical contacts dies out. An ESD induced glitch may occur deep within the system registers or memory and if there is a check method to validate the action, then the system robustness can be improved by ignoring and recovering erroneous transient events by executing one or more "second opinions" about the validity of a state before acting.

3. The examples above describe ESD/EMC immunity. However, similar techniques are related to EMI emissions management for low level operations which need detailed controlling and planning. For example, if a system has internal and external memory in use, there may be a high difference in power consumption between the two blocks. Accessing each block for a relatively long time before alternating to the other one may create long periods of high and low power consumption. In a battery operated component, these alternating periods may create long voltage drops, which may complicate the supply

design. But if the high current and low current memory accesses can instead be rapidly interleaved without affecting the component performance, then current pulses may be minimized and these EMI inducing transients may be easier to mitigate with less expensive bypass capacitors and filtering. Other functional blocks may also be considered, including interleaving high current functions such that the system does not transition rapidly from "all on" to "all off", but instead keeps a consistent allocation of load versus time.

These three examples vary in the type of transient robustness or immunity being addressed, but share similarities in the use of software to mitigate the issue. The concepts are usually straightforward, but the implementation depends on the complexity of the system software. Direct access and control over system states can be easily handled in a small microcontroller based component or even an advanced real time operating system (RTOS). But virtual machines and multitasking operating systems may impede the ability to actively monitor sequential system states to detect transient events on a discrete time scale, limiting the opportunities for software recovery methods.

3.3 Comprehensive Co-Design Methodologies

On a long enough product cycle with sufficient product value at risk, 3D modeling of ESD/EMI design becomes viable. A one-shot deep space probe simply doesn't allow for an iterative product development cycle. “Lessons learned” may result in an inoperative probe. In such cases, the aggressor discharge strike might not even be reproducible in a development lab, and the actual environment may only be created and tested in a simulation.

Another case is when the product has a very complex mechanical and circuit design and has limited options for on-board protection. This is especially true in the RF area which often requires 3D simulations to optimize the RF performance and ESD robustness.

Over time as computing power increases, the simulation algorithms improve, and costs decline, this “brute force” methodology may become the obvious choice for any designer.

Of course, any simulation is only as valid as the models and conditions applied, but many areas of design utilize this methodology exclusively. Nodal circuit simulation environments like SPICE are mature and widely available, but while models of ESD simulators are well known and published, and the circuit elements are well characterized in the frequency domain for EMI and signal integrity analysis, there are few resources for out-of-the-box high-current/fast-transient ESD models of TVS, ASIC and even passive capacitors and inductors/filters.

Simulation is thus the foremost shortcoming of the present-day state of the art in achieving ideal ESD/EMI co-design, and these factors are expanded upon more fully in Chapter 5.

3.4 Conclusion

The chosen methodology from Table 2 is ultimately selected by the designer as a compromise on an optimum fixed point in a “tradeoff gamut” between three generally conflicting goals: (1)

ESD/EMI robustness and susceptibility resistance, (2) signal integrity and functional performance (bandwidth, data-rate, minimum emissions for example), and (3) cost and time to market.

The distinction between Basic, Advanced and Comprehensive methodologies in this chapter is defined by the complexity and effort required of the method as well as the ability of the underlying model to predict robustness of the system. In addition to this depth of complexity, the breadth of design methods is primarily divided into practical analysis and theoretical simulation.

Complexity does not always imply improved robustness, however, and in some cases the most basic shielding design of a product enclosure can deliver the highest system level robustness for essentially no additional product cost or development time. Alternatively, expensive simulation environments utilizing component models which are inaccurate in the ESD domain may indicate the need for costly and unnecessary additional components, redesign delays, and expensive silicon spins, and result in a less robust system than expected. This chapter explored the prevalence and cost-effectiveness of the different methods as well as the ESD performance of the results that can be expected.

Within each method, critical exposed and susceptible nets must be identified and assigned reasonable and sufficient robustness levels. Aggressor pulse entry (conducted, induced) points for hard- and soft failures should be outlined. Component selection, layout and placement should be considered with regard to ambient and direct ESD/EMI strikes and disturbances and the effect on signal integrity. System partitioning, grounding, clamping, shielding and return path shaping are also considered, along with the problems of hidden potential multiple/secondary discharge points within the system.

By managing these issues in the concept, design, and prototype phases, a designer can observe and improve the extent and effectiveness of any element or flow in a process intended to balance ESD/EMI robustness, performance, and cost with existing and emerging methodologies.

References

[1] Industry Council on ESD Target Levels, "White Paper 3 System Level ESD Part I: Common Misconceptions and Recommended Basic Approaches," December 2010, at www.esda.org or JEDEC publication JEP161, "System Level ESD Part I: Common Misconceptions and Recommended Basic Approaches", www.jedec.org

[2] Laasch, Ingo et al, "Latent Damage due to multiple ESD Discharges," EOS/ESD Symposium, 2009, pp. 1-6

[3] Hua, Vanessa, "Sparks over static: An age-old problem still vexes makers of tech devices," San Francisco Chronicle, August 27, 2001

[4] Frei, S.; Wu, W.; Hilger, U.; Edenhofer, J.; Stecher, M.: "Packaging and Handling Test according to ISO 10605: How comparable are tests with different ESD generators?", ESD-Forum 2007, Munich, Germany, 2007

Chapter 4: Reference Methodologies for IC/System Protection Co-Design

Harald Gossner, Intel Corporation
Guido Notermans, ST-Ericsson
David Pommerenke, Missouri University of Science & Technology
Benjamin Van Camp, SOFICS

4.0 Introduction

SEED was introduced in White Paper 3 Part I as a method enabling board designers to develop an ESD protection concept based on ESD specific models for all elements involved in the ESD discharge path. Here in Part II, a 'divide and conquer' approach is chosen, where the various failure mechanisms are classified and the appropriate design and testing methodology for each category is described. Many detailed aspects of this methodology are still to be developed. The purpose of this description is to give a common base for discussion and to provide a setting for direction.

The first step of analysis is to determine the discharge path tree to be considered. The path can be traced from the entry point of the pulse. There are various ways to force the IEC gun stress pulse to the system. A system consists of a case, the PCB including external ports and the electronic components thereon. Usually a contact mode IEC 61000-4-2 discharge is applied to all metal housing parts. The IEC 61000-4-2 air discharge is applied to insulating cases or parts of it as described in Chapter 1. In the latter case, pulse energy can be coupled to the board either by electromagnetic fields or by sparking to some metal parts. The metal parts guide the waves and both fields and currents can reach the board. From that point of view, air discharge and contact modes are similar. The focus of the SEED concept is on measures which are implemented on the PCB. Mechanical design aspects of the system regarding shielding and avoidance of secondary sparking are not treated by the SEED method.

We will first start by introducing a series of SEED categories through examples which will be categorized by the impact ESD has at the system level. An example of an ESD event which can be covered by the SEED approach is a discharge to metal pieces which are galvanically connected to the wiring of the PCB. This can be a PCB port which is hit by a contact discharge (like a cable discharge event), a portion of an audio or USB jack which picks up energy from a nearby discharge to the ground shield or a part of the metal connection to a discrete component of the system (like an ear piece or a keypad of a mobile) where the discharge can occur through gaps in the case. The effect of the system level ESD event on the pin(s) that are galvanically connected to the metal which is zapped will be called a SEED Category 1a event; it addresses physical damage from discharges to external pins.

From the entry point the energy can spread along the direct metal connection to an IC pin. The energy is shunted through PCB protection diodes and IO circuitry (including on chip ESD protection) to VSS and VDD nets of the IC and PCB (See Figure 11). Category 1b is a slightly different case: it involves other paths which can lead to damage to pins which pick up a high energy pulse without being directly (galvanically) connected to the outside world.

Alternatively, part of the charge might be forced into the substrate of the IC at any pin, which can cause latch-up events or upset errors. This type of path is assigned to Category 2.

Parallel to the current in the galvanic network connected to the entry point, a small part of the energy might be coupled to neighboring wire lines of the PCB by mutual inductance and capacitance or can be picked up from electromagnetic (EM) radiation by PCB traces acting as an antenna. The induced pulses can travel in these parallel metal networks and be shunted at IO pins or dedicated board shunt elements like TVS diodes to VDD and VSS nets. Such an induced pulse of low energy is not able to create damage directly due to its dissipated energy, but it might cause an upset or other malfunction of the system. Also, as VSS and VDD nets on an IC or even on a PCB might not represent an ideal sink, the pulse energy can penetrate at low energy levels throughout the whole system as supply noise. Additionally, disturbances of the signal lines at this low level of energy can degrade signal integrity. These disturbances can even pass a first IC and be transferred to another IC which it is electrically coupled to. All these mechanisms, related to rather low energy levels of the stimuli initiating the fails, are part of Category 3.

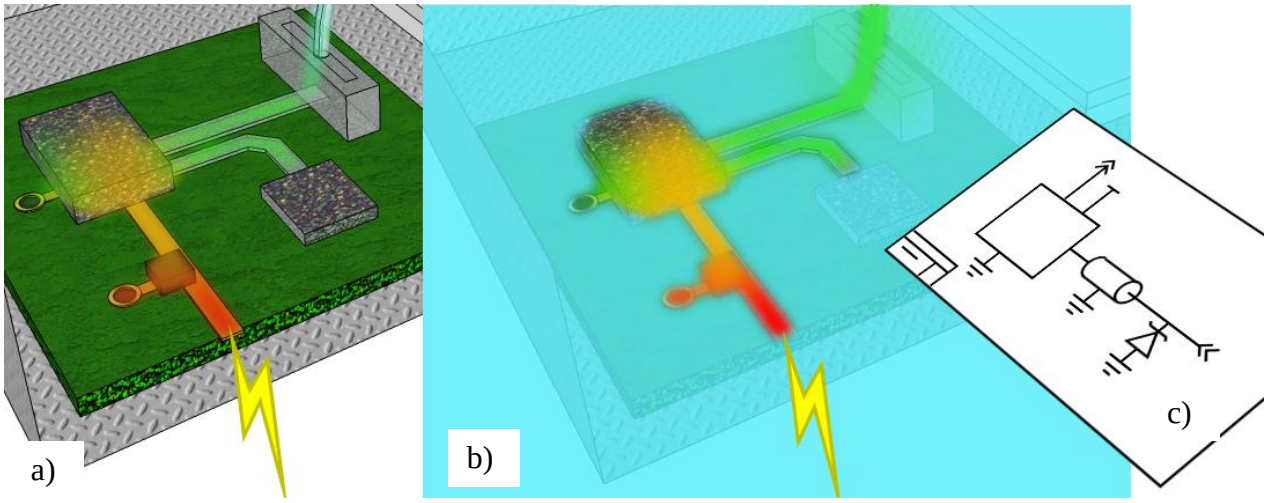


Figure 11: Qualitative illustration of system ESD discharge along PCB lines and typical protection concept: a) PCB b) highlighted discharge paths and c) related circuit block diagram

As discussed in Chapter 3, applying an IEC ESD pulse to an encapsulated (end)-system, to the PCB only or even to single ICs, usually leads to very different discharge paths and failure mechanisms. There is a need for sub-component characterization to achieve a cost efficient solution for the final system while maintaining short design cycles. SEED provides a very good direction for optimization of ESD protection of certain PCB paths. This design solution can actually be verified by system level ESD tests on a PCB level for specific paths or by other stimuli of high energy pulses like TLP. This intermediate test is a valuable step in the system development process and provides a good basis for the qualification of the final system, if design measures for shielding and prevention from secondary discharge are taken into account properly. At this point it should also be mentioned that the SEED concept can be equally applied in cases where the main ESD discharge path leads through the IO circuit, such as in the case of no TVS

diode protection. Though having no TVS protection is discouraged due to soft fail risks and RF performance constraints it might be a viable solution for some applications.

4.1 Approaches – Categories

4.1.1 Categories – Definitions

In summary, the previous discussions can be rolled up into the following SEED categories:

SEED Category 1:

a) External pin experiences hard failure due to a direct ESD zap (failure root cause: high pulse energy at exposed line)

b) Non-external pin experiences a hard failure due to an indirect ESD zap (failure root cause: high transferred pulse energy to non-exposed lines)

SEED Category 2: Pin experiences a transient latch-up event which can lead to either a hard or soft failure (failure root cause: current injection into the substrate which is too high)

SEED Category 3: Describes protection of an IC experiencing soft failure due to low amplitude transient bursts in the system during an ESD zap (for example, this may be caused by degraded signal integrity of an exposed line or cross-talk to a neighboring line or supply noise).

Note that for Category 2, if the part is powered up, the energy delivered by the supply can be the source of the damage. For example, if the supply dumps a current which is too high for a longer duration in the low ohmic path created by the latch-up event, damage will occur. For SEED Category 3, failures can only be seen if the system level pulse is applied when the component is powered up.

4.1.2 Category 1

The SEED Category 1 approach focuses on physical damage and higher energies and is not really intended to reduce soft fails. When the energy of an IEC 61000-4-2 discharge is coupled into a PCB line connected to an (external) pin, the main ESD current typically flows directly to ground through the on-board TVS. Nevertheless, some residual current will enter the connected IC pin and flow through its internal protection to ground (see Figure 12).

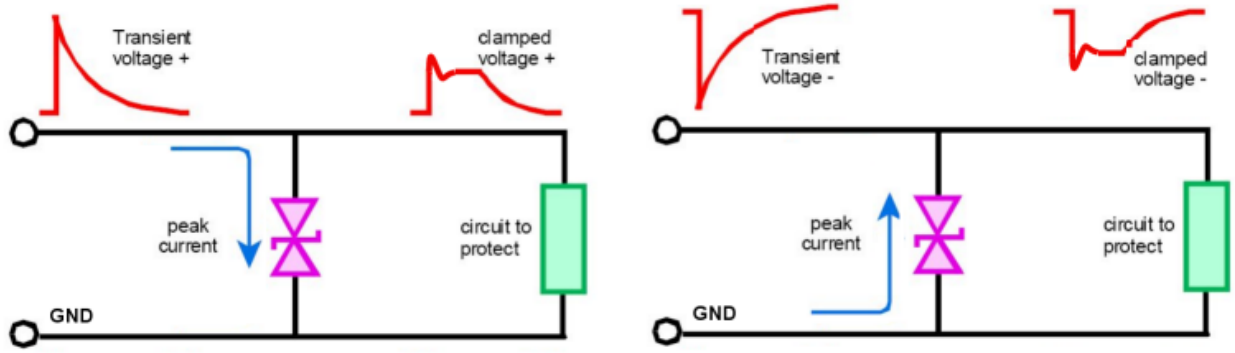


Figure 12: During an IEC discharge to an external system pin, the main current flows through the on-board TVS protection to ground, but some current will enter the IC and flow through its ESD clamp to ground.

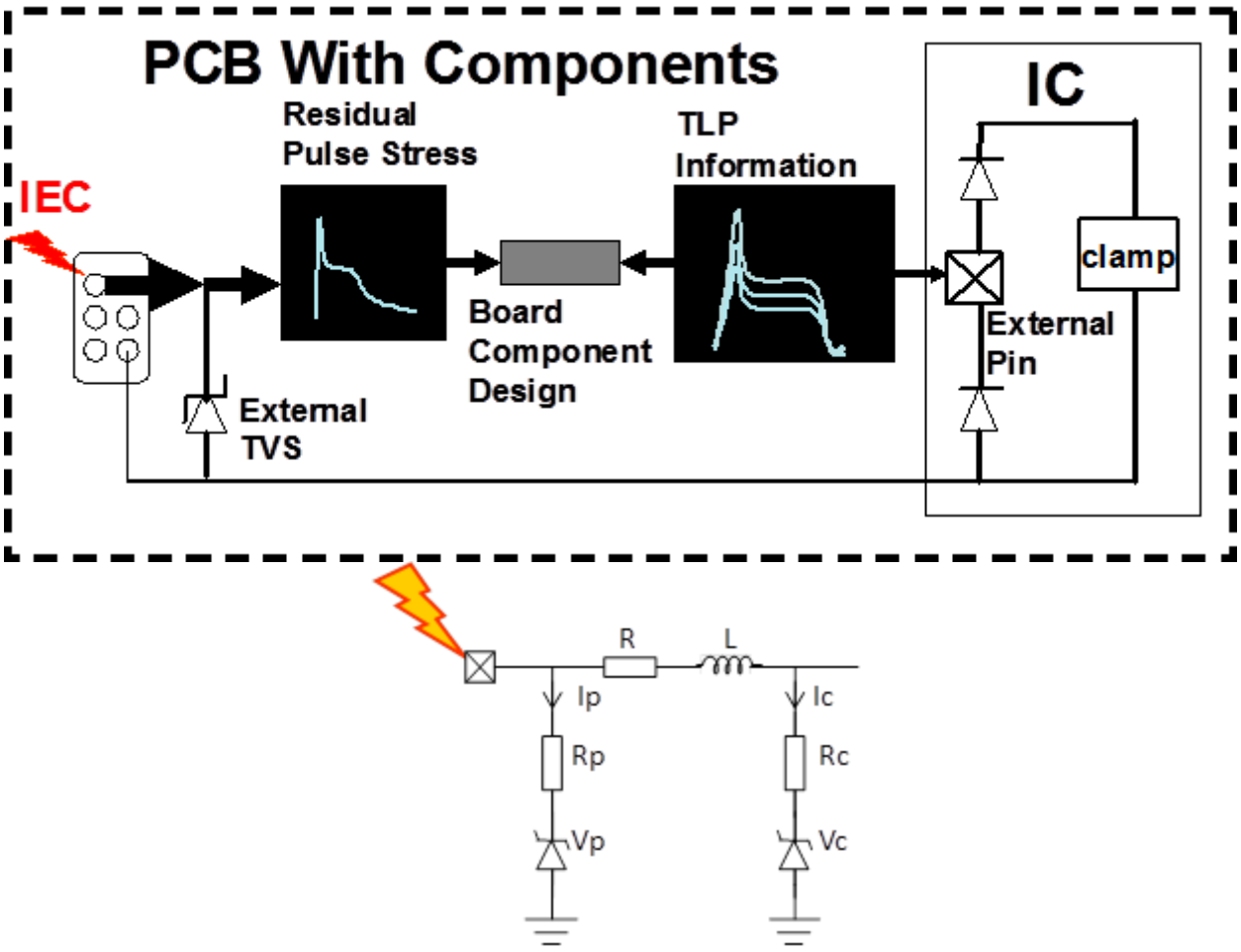


Figure 13: Simplified replacement diagram showing the essential components of a basic SEED concept [26]

In order to prevent damage to the IC, off-chip protection is often added as shown in Figure 13. It is important to assess the amount of current (Ic) which may enter the IC and the associated (over-) voltage (Vc) across the connected IC circuitry.

To analyze the residual pulse and the optimization of the PCB protection, three basic SEED approaches of increasing complexity might be chosen depending on the system conditions. If the protection can be configured by fast and low ohmic breakdown elements like some TVS diodes and high ohmic resistors (in the > 10 Ohm regime), a quasi-stationary model allowing a back-of-the-envelope estimation of the required parameters can be applied.

In most practical cases, complex impedance plays a major role involving inductance of wiring and discrete capacitors. This requires a more detailed transient approach. Still, a transient model of the IC pin itself is not always needed due to the suppression of fast transients in the PCB network [1, 2]. Characterization of the IC and simulation effort can significantly be reduced by this simplification.

However, in cases where a matched network without clamping elements allows fast transients to travel to the IC pin without significant damping, transient models of all elements of the path including the IC IO circuit have to be considered.

In case of a quasi-stationary model the calculation may be simplified by approximating the TVS and the on-chip protection by ideal zener components, characterized by their on-voltage (Von) and on-resistance (Ron). A simplified replacement diagram is shown in Figure 13. If all parameters of the components in Figure 13 are known, a straightforward application of Kirchhoff's Current Law will yield the current distribution (Ip, Ic).

This approach does not reflect the actual behavior of the system of TVS diodes and IO on chip protection, as these are competing elements with characteristic transient responses. It is important to realize that the on-chip protection might need to take the first transient, such that the combined effectiveness of on- and off-chip protection needs careful consideration. If the on-chip protection shows snapback behavior, it is possible that the on-chip protection takes all the current, before the off-chip protection triggers. For the RC-bigFET approach, the current conduction capability is time-dependent, with potential triggering and/or turn off issues. However, for the sake of a PCB design decision, a worst case scenario requires a robust protection concept. In the case that the IO circuit gets into the low ohmic state first, turn on of the TVS diode might be an issue. The PCB design has to account for this and the assumption of a low ohmic/high current I-V characteristic is appropriate. Still, the assumption of an effective turn-on of the TVS diode without delay is an optimistic one. In real cases there will be an initial overshoot, which may already damage the IC. Therefore, the methodology of comparing quasi-stationary I-V characteristics only applies to very fast triggering components, like TVS diodes, with small overshoot plus the use of filtering elements on board between the TVS and IO which blocks fast transients in the sub-ns regime. PCB traces may serve this purpose. Note that if the system level test is performed with the component in a working mode (supply lines charged), the characterization of the ESD cell must be performed with a biased supply line in order to give relevant data.

The resistance R and inductance L of the wiring, both on-board and on-chip, play an important role. The total inductance between the shunt elements, comprised of trace, interconnect, and bond wire inductance, may reduce the current from the first peak entering the chip to a negligible value. In that case, the IEC robustness may be estimated by considering the current distribution in the second peak only. Since the timescale of the second peak is very close to the HBM timescale (around 100 ns), the relevant I-V characteristics of all components may be estimated using a standard TLP test.

4.1.2.1 Safe Operating Area (SOA)

Using the simplified basic SEED model depicted in Figure 13, calibrated with 100 ns TLP characterization data, the residual current into the IC and the ensuing pin voltage may be calculated for any given on-board resistance R (R_{on}). Figure 14 shows Vc and Ic assuming no additional board resistance R exists. In that case the 'operating point' of the on-chip supply clamp during a system level ESD discharge (Vc, Ic) turns out to be outside the SOA for the output domain on chip, which is defined by the design target for the clamp. The SOA is bounded by the maximum ESD current for which the clamp is designed, such as Imax = 4 A TLP (~6 kV HBM voltage), and the maximum voltage on the core circuitry before oxide damage will occur, such as Vmax = 11 V (oxide breakdown of a thick oxide transistor).

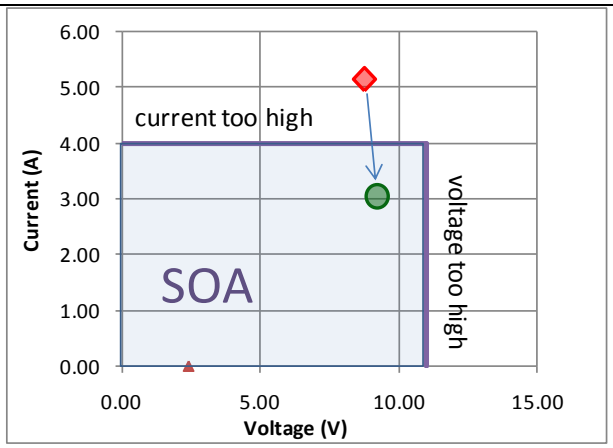


Figure 14: Increasing the series resistance on-board by 1 Ω moves the output 'operating point' (Vc, Ic) during an 8 kV IEC discharge into the SOA [26].

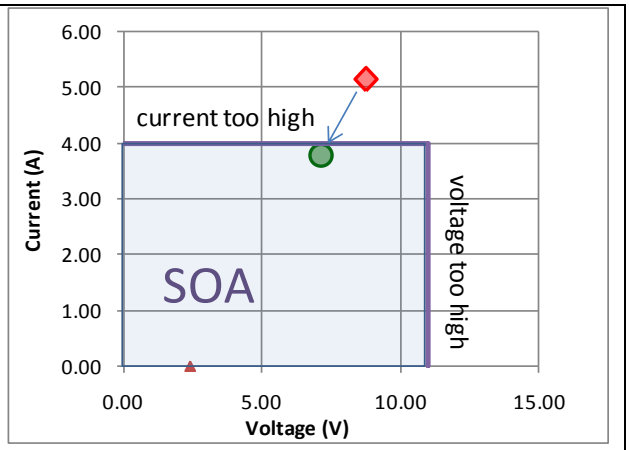


Figure 15: Choosing a different TVS with Von= 6 V and R_{on}=0.1 Ω moves the output 'operating point' (Vc, Ic) during an 8 kV IEC discharge into the SOA [26].

The SOA approach allows assessment of possible improvement measures. For instance, by increasing the on-board resistance R, the current into the supply clamp may be reduced. However, in many cases, such as the case of an audio output, the required efficiency of the power stage usually does not allow increasing the output impedance. An alternative solution is to find another TVS which has either a lower on-voltage or a lower on-resistance. Figure 15 shows that by using a TVS with V_{on} = 6 V and R_{on} = 0.1 Ω, the output (Vc, Ic) point moves into the SOA. Increasing the holding voltage of the on-chip protection or designing the IC to allow a larger current to flow through the on-chip protection, are alternatives.

V_{on} cannot be lower than the maximum operating voltage of the output (in normal operation) plus some margin. So, the easiest solution is to find a TVS with a V_{on} as low as possible and a sufficiently low R_{on}. To cover transient behavior due to impedance of the PCB network, package and protection elements, an extraction of resistor/inductor/capacitor (RLC) models of these elements at high currents is required. One example is the behavior of ferrite beads, which are widely used to suppress high frequency surges reaching sensitive pins. It has been shown that their damping behavior is strongly dependent on current amplitude and needs to be extracted such as through high current TLP pulsing [1, 2].

The simulation approach also includes transient models representing the turn-on behavior of the PCB protection elements at fast pulse rise times (or at high frequencies). Preferably these should be delivered by the component supplier. However, if needed, the characterization can also be done by the PCB designer using TLP equipment with a fast pulse rise time (typically < 1 ns). Finite turn-on time and package inductance of the protection elements such as PCB voltage clamps (i.e., if it is a varistor, but also capacitors) lead to voltage overshoots and will strongly impact the effectiveness of the ESD protection strategy. It is important that the transient response of any off-chip protection is characterized for these fast pulse slopes. Regular TLP measurements have a rise time of 10 ns and pulse duration of 100 ns. Typically the voltage shown in the TLP I-V curve is an average of the voltage measured between 75 ns and 85 ns, that is, near the end of the TLP pulse. It therefore lacks information of what the voltage is during the first part of the pulse. Furthermore, a rise time of 10 ns is too slow to characterize the overshoot during very fast ESD events. Some TLP systems allow changing the setting to faster rise times. To correlate with the fast transients of an IEC event, a rise time of 400 ps is a good typical value. The extraction of the voltage waveform as the component responds to a fast risetime pulse is the basis for an effective analytical design methodology.

The RLC network of the PCB and package can be extracted from standard 2.5D or 3D EM simulators solving Maxwellian equations. 3D simulations are especially slow, however, and only a few paths can be analyzed in a reasonable time frame in real life.

IC pin models need to reproduce the breakdown characteristic and the on-resistance of the discharge path through the IC as well as the I_{t2} where a transistor enters its second breakdown region and is irreversibly damaged. Transient turn-on behavior of the IC IO circuit is not relevant as long as the network damping is significant (Note that in some cases lumped capacitors might create non-negligible transient effects) [1, 2]. This reduces the effort in characterization and, even more importantly, avoids convergence problems and misinterpreted current distribution due to competition between the IC circuit and a PCB protection diode. Accepting the IO IC protection in the on-state usually results in a worst case condition for the current distribution and allows safe guidance for the optimization of the protection circuit. If transient effects have influence on the triggering of the on-chip protection (as explained above), these need to be taken into account.

A possible flow of a transient simulation of the PCB optimization for system level ESD protection is described below:

1. Extract the netlist of board (RLCk or S-parameter) from the PCB layout data
2. Import the electrical board netlist to a network simulator program
3. Add discrete PCB elements (TVS, resistors, inductors, ferrites, capacitors) to predefined nodes of the board schematics
4. Add IC pins to the board schematics
5. Bind high current models to IC pins and discrete PCB elements
6. Perform a simulation using ESD stimuli
7. Assess fail criteria at IC pins (and discretes)
8. Select better discrete device (TVS, R, L,…) if necessary
9. Optimize placement of discrete elements (go to 1.)

4.1.2.2 Design Verification Using Very Fast Transmission Line Pulse (VFTLP) Data

In the previous examples, the specific transient response of an IC IO circuit to initial overshoots of the residual pulse passing though the PCB network has been neglected. In most PCB networks this is a valid approach, as the overshoot is reduced by the damping of the PCB network. However, in the case where the fast pulse passes the PCB network and generates a large overshoot at the IC IO, the described methodology doesn't meet the real situation. Even though the short duration of the overshoot generally shifts the failure current to higher values, damage can still occur. If the circuit doesn't turn on in time, the increased voltage may lead to a physical fail.

To extract the ESD behavior realistically, a VFTLP characterization of the IC IO circuit provides the relevant information needed. A VFTLP system with a 2 ns pulse width and 400 ps rise time is well suited for (typical) characterization of the IO circuit in terms of turn-on, on-resistance and I_{t2} of short pulses with very fast rise times. This might be applicable for antenna ports for example.

To include the results of VFTLP measurements for specific PCB traces, the following procedure is given as an example. It is assumed that the off-chip protection is chosen according to the principles discussed previously. VFTLP will enable extraction of the voltage overshoot of the off-chip protection, as well as the I-V curve for the on-chip protection. Using Kirchoff's laws, one can check whether the current flowing through the IC is sufficiently low enough to avoid damage similar to the basic SEED as discussed in Section 4.1.2.1. If not sufficiently low, the impedance of the connection can be modified to lower the current peak through the IC. Other measures include faster off chip protection, additional series resistance in the connection, better on-chip ESD protection or parallel capacitance.

General trends for the choice of capacitance and inductance are:

- Higher parallel capacitance lowers voltage.
- Higher series impedance/inductance (such as in IC packaging lead wire) reduces current

The interaction between two or more components on board can cause residual pulses to vary dramatically when the pulse energy is shared between different types of clamps over non-negligible electrical distances. For example, a polymer component may clamp an IEC pulse at 30 ns very well when tested on its own. The initial voltage peak helps to trigger the component and shunt the current effectively. However, if it is placed in a circuit parallel to a very fast silicon shunt component which has a lower clamp voltage and lower failure threshold, then the silicon component may inhibit the polymer component from triggering, and the "protected" IC will fail at unexpectedly low system levels.

In this case the "DUT" becomes the entire system of nodes on the IO line under inspection. The VFTLP or any chosen stress pulse has to be applied to the actual system or equivalent evaluation board with all TVS and auxiliary bypass components installed.

Another transient aspect is the turn-off behavior of the RC-triggered on-chip and off-chip protection. If sufficient energy is left in the late phase of the pulse when either protection component turns off, damage can occur. Though this effect is not very common, it is still important to understand the turn-off behavior of these protection components.

4.1.3 Category 1b

Category 1b, protection of a non-external pin which experiences a hard failure due to an indirect ESD zap (failure root cause: high transferred pulse energy to non-exposed lines), is described below.

There are well reported entry paths for such indirect zaps. One way they can occur is by sparking from nearby connector pins or from parts of the housing to PCB traces connected to these pins, or breakdown of isolation between neighboring PCB lines or package balls. Also, discharge through gaps in the case can lead to stress of non-external pins. In very specific cases, like flex cables connecting modules in the system, very strong electromagnetic coupling can result in a destructive fail at a non-external pin.

One approach is to add off chip protection to lines that are *likely* to see a high energy induction. Capacitors and filter elements can be used as well. Effective capacitors have to be dimensioned sufficiently large to avoid acting as *temporary* storage components, which then release charge in very short timeframes. The term 'likely' is hard to define, as it requires PCB and system analysis. Of course some examples are:

- Traces that connect to flex cables or other board-to-board connectors
- Traces connecting to user interface devices like a liquid crystal display (LCD) or keypad
- Traces that have long parallel runs with high noise traces (like running parallel to an audio line which connects to the outside)
- Reset lines that are routed over many boards or on board edges
- Power Good lines that go to a power supply
- JTAG lines often cause trouble
- LCD connection lines as they connect to flex cables
- All lines that connect to user interface devices like knobs

Pins in Category 1b need the same protection approach as the pins in Category 1a, although the pulses used for IC characterization might be slightly different, as explained in the examples below.

The suspicion that the transfer of relevant (destructive) energy by inductive or capacitive coupling between PCB traces has been proven to be very unlikely by recent investigations [3]. In this case the waveform of the induced pulse is typically short (up to a few ns), but can reach high current levels (up to 2-3 A) [3, 4]. It is assumed the pulse is capacitively/inductively coupled into the line, such that lowering the capacitance between the lines shortens the pulse and lowers the amplitude. The need for good design in this respect is higher for pins with low CDM withstand levels for example.

The response time of off-chip protection can be of importance. As in Category 1a, VFTLP like measurements (as well as any TLP measurement with fast rise times of ~400 ps) should provide sufficient information. Note that the rise time and pulse duration of the event seen by the pin is largely influenced by the amount of coupling between the exposed (aggressor) and non-exposed (victim) lines, such that careful board design can help to reduce the requirement for fast and highly robust on-chip ESD protection.

Further system level ESD design considerations are similar to those for EMC design; the goal for both is to limit the amount of current/voltage/energy transferred to non-exposed lines. This prevention of ESD stress from reaching the IC is addressed by the advanced SEED concept and can be assumed to be a common design practice for EMC robustness.

4.1.4 Category 2

Protection of any pin experiencing transient latch-up which can lead to either a hard or soft failure (failure root cause: current injection into a substrate which is too high) is described below.

Overstress to any pin of an IC can result in latch-up. Overstress includes surges above the power supply voltage, below GND to a supply line, and current injection into an IO pin.

The phenomenon "latch-up" and a qualification methodology for latch-up robust products is defined reasonably well in JEDEC standard JESD78D of 2011 [5]. Historically, latch-up covers product fails which result from the occurrence of low-ohmic paths, caused by overstress, which triggers a parasitic pnpn or npnp clamping component. To account for this, all ICs have to pass JESD78D latch-up testing during qualification.

The stress defined in JESD78D has a rise time (t_r) of 5 µs–5 ms and pulse duration of 2 × t_r to 1 s. Compared to typical ESD events on an IC or system level, these pulses are very slow, thus, JESD78D is often referred to as a "static" latch-up test. However, it is well known from several examples that transient latch-up (TLU) can occur if only a small part of the IEC energy pulse reaches the IC. TLU can occur in products during IEC testing or even in the field although they passed the JEDEC latch-up qualification test. This effect and its physical root cause have been intensively discussed in literature [6-24]. The reasons for the fails are surges which are (much) faster than the pulses defined in JESD78D. Such surges can occur during system level stress. Working Group 5.4 of ESDA is presently reviewing this topic and plans to release new recommendations as a Technical Report (TR) toward the end of 2012.

At the time of this white paper writing, the WG5.4 TR covers about 20 different examples of transient latch-up fails from business applications of digital circuits/processors, mobile devices, automotive, high-voltage circuits, and analog circuits (audio and power management). Those examples are now categorized with respect to a possible test methodology to reproduce the fail. Basically, there are two classes of TLU events. In the first class, the latch-up event can be reproduced by JEDEC JESD78D testing with increased compliance values. Of course, it is not straightforward to just increase the compliance values of JESD78D without changing the pulse width, as it may result in EOS damage of the IC. In the second class, transient latch-up can only be reproduced by transients with rise times significantly shorter than the JEDEC JESD78D surge. Thus, for both classes a pulsed methodology based on square pulses could possibly work; discussion has started. The final goal of the ongoing work is to determine the appropriate emulation of stress and failure signature by TLU testing.

Once the IC has been characterized up to a certain TLU current threshold on relevant IO pins, this information can be used to detect critical excess current, when injection of a system level ESD pulse to the PCB network is simulated. The simulation has to take into account inductive or capacitive coupling between PCB traces, which can spread ESD pulse energy to various parts of the PCB network attached to IC IOs. PCB design measures as part of an advanced SEED co-

design concept must be taken to limit the current at IOs to a safe level below the characterized TLU threshold.

4.1.5 Category 3

Category 3, describes protection of an IC experiencing soft failure due to low amplitude transient bursts in the system during an ESD zap (for example, this may be caused by degraded signal integrity of an exposed line or cross-talk to a neighboring line or supply noise).

Failures of Category 3 are diverse and could be triggered by a very low fraction of the ESD pulse. The underlying causes of soft failures are often not known. Often times, indirectly coupled ESD currents are ringing signals having ring frequencies from tens of MHz to a few GHz. Not only is the ringing frequency determined by resonances of the enclosures, wiring and PCBs but also by the spectral content of the specific ESD generator model used. Each test point might have its own resonant coupling path and each ESD generator model has its own spectral content leading to larger variations if the same DUT is tested for soft failures by different ESD generators [25].

However, one can categorize soft failures by different criterion:

1) In-band / out-of-band with respect to voltage. For an in-band error the noise voltage needs to be larger than VSS and less than VDD, or, for differential signals, within the allowed common mode and differential mode voltage swing range; thus, within the normal operating range of the input, otherwise it is called out of band. In general, in-band errors (with respect to voltage) add noise and cause signal integrity violations, but the voltages stay within normal operating limits. For an output, the current forced into the output needs to be less than the maximal allowed current, and the voltage at the output must be maintained within the normal range of voltages. Most in-band errors are caused by voltage changes that allow noise to be confused with legal data. If, for example, the ESD causes the common mode level of a differential mode signal to swing up beyond the maximum common mode range of the differential input, then this would be considered an out-of-band soft failure with respect to voltage.

   If the common mode would swing below VSS or above VDD, then the ESD protection circuit can inject currents into VSS, VDD or the substrate.

2) In-band / out-of-band with respect to pulse width. If the intended minimal pulse width is, for example, 2 ns and an ESD pulse with 2 ns width arrives at the receiver, the receiver will confuse the ESD induced voltage for valid data. Such a pulse is considered as an in-band signal with respect to pulse width. However, if the same receiver is able to react to a 200 ps wide pulse, although the fastest system signal would have > 2 ns pulse width, then the 200 ps receiver can react to the 200 ps pulse. Such a pulse is considered as an out-of-band signal with respect to pulse width, as its width is narrower than the narrowest intentional pulse within the system. These types of errors are very common for reset and other status lines, as the input buffers are often much faster than they need to be. Together with long traces or poor routing of status lines over connectors, for example, strong coupling paths are formed between the ESD pulse and the receiver, causing the receiver to react to a very narrow pulse. Low pass filters at the IC input can help to improve the situation.

3) Local vs. distant errors. A local error is caused by changes in the IO buffer which receives the ESD; a distant error is caused by changes far away from the IO buffer that received the ESD. For example, if a negative pulse opens a p-type/n-type junction (PN) diode and leads to an injection of charge carriers into the substrate, and this current disturbs a crystal oscillator (XTAL) input pin at a different IO, then this would be considered a distant error. The same is true for a positive pulse injected into an output which forces current into VDD. This current leads to voltage drops within the VDD system and can cause an error at a level translator, or a phase lock loop (PLL) away from the output.

4) Amplified / non-amplified soft failures. Amplified soft failures involve transient latch-up or the trigger of power clamps, while non-amplified soft failures are caused by voltage changes, IR drop, or cross coupling without triggering high current devices. Ringing pulses can lead to fast transient latch-up. A fast transient latch-up can have many different consequences, from increased current consumption with no direct effect on functionality, to increased current consumption with soft failures, to destruction of the IC. Another example of an amplified soft failure is the trigger of a power clamp. This can again have multiple consequences. If the holding voltage is higher than VDD, the power clamp will recover after some time. During this time, the ICs logic can be disturbed, but the IC will survive. If the holding voltage is below VDD the IC will try to pull VDD down. Depending on the power supply this can destroy the IC.

It should be noted that fails in Category 3 are often resolved by modification of software. This is also possible to a certain extent for Category 2 fails. The hardware aspects are addressed by the advanced SEED approach.

4.1.6 Pass-Through Effects

While in most cases the semiconductor component suffers from a hard or soft fail once its pin is hit by the ESD residual pulse, in some cases the part only acts as transfer gate into another network, where a subsequent element might fail. A typical example is the front end module attached to an antenna where a portion of the ESD energy from the antenna pin interface can be transferred to a surface acoustical wave (SAW) filter, which can only sustain a certain overvoltage. To account for this, a characterization of the ‘transfer’ or better ‘blocking’ capability of the first component is required. This is applicable to only a few, mostly well-known components, and is not covered in the SEED characterization above.

4.1.7 Summary

In conclusion, the failure mechanism and protection methodology of failures in Category 1 are addressed by the basic SEED concept as introduced by White Paper 3, Part I [26]. Failures of Category 2 and 3 need different analysis and protection methods which require an advanced SEED approach. This comprises the characterization of the sensitivity of the IC against low energy level pulses. This is partially overlapping with EMC considerations, but is not identical, as the typical effect addressed herein appears in the time domain, while EMC analysis is typically done in the frequency domain.

4.2 Examples

4.2.1 Category 1a

4.2.1.1 Voltage Waveform Extraction

Voltage waveform extraction can be done with VFTLP measurements. As the incident and reflected waveforms do not overlap, the waveforms contain all information necessary to extract the overshoot information. The key elements of the VFTLP which make it useable for this purpose are:

1. The ability to produce fast rise time pulses
2. The ability to measure the response accurately

Some portion of the fast transients can reach the component when the transmission line between the source and component matches. One example of fast transients can be seen in Figure 16. The IEC contact discharge current waveform is measured just before an IC component on a small size printed wiring board (PWB). The current moves through an 8 cm long trace through the component into the board ground. The PWB is placed on an IEC test bench close to the electrical ground and is grounded through a high impedance ground cable. The fast transients will stress the component when the PWB is capacitively coupled to the plane of the IEC bench electrical ground and the rest of the charge will dissipate through the grounding cable within the next 500 ns.

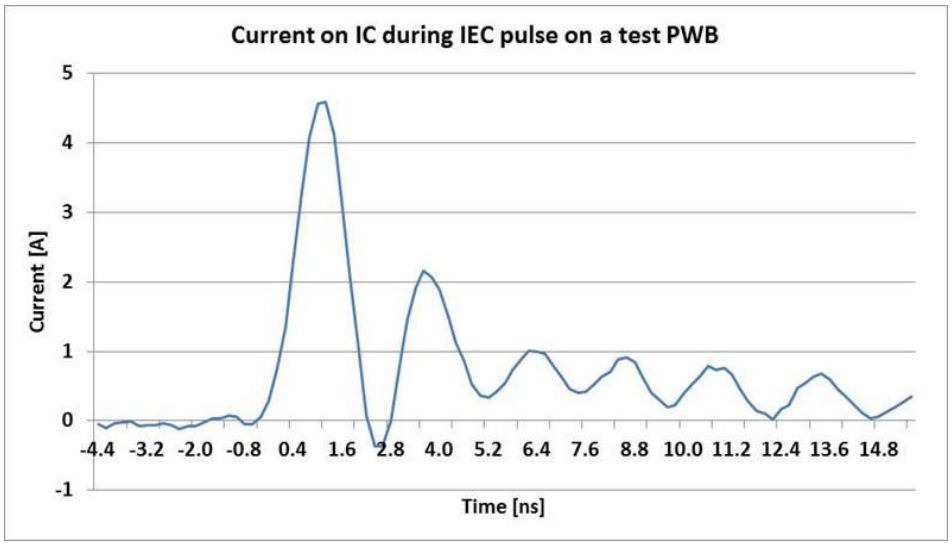


Figure 16: IEC contact discharge current waveform is measured just before an IC component on a small size PWB [26]

4.2.2 Category 1b

4.2.2.1 CDM as a Robustness Indicator

Today, there is no accurate information available about the robustness of an IC pin for Category 1b failures. As the expected waveform entering the pin is somewhat CDM like, it is tempting to use the CDM value as a predictor for this case as well, especially if the CDM peak current level is

available. For Category 1b, it is estimated that about 3 A (typically) should be shunted, which is normally below the peak current of the CDM pass level. If not, this pin should be considered critical, and the addition of off chip protection is recommended.

Using CDM as a predictor for Category 1b might be tempting, but it comes with many pitfalls:

1. CDM is a one pin test, while in system level stress two or more pins are involved.
2. Pulse rise time in a CDM tester is always faster than when the component is soldered on a PWB with additional board parasitics.
3. As said, in the system level case, the IC can be powered up, which can lead to destructive or non-destructive transient latch-up. This type of failure is not covered in the CDM case.
4. The CDM data does not provide any information on whether or not the IC remains functional during or after the event. Rebooting might be required, even if the IC passes the highest level of CDM.
5. The CDM level is dependent on the IC and package size; larger components see more ESD current for the same CDM level. This is not the case for the system level event. Therefore, from a system level point of view, for the same CDM performance, a large component is more robust as compared to a small component though the above notes about transient latch-up and functionality must be considered as well.
6. One more thought on polarity - If we look at positive and negative polarity and compare CDM to pin injection into an IC that is mounted to a board, the current on the pin might be the same, but the current on the other pins is not the same, as the current will exit the component mainly on VDD or VSS, but possibly also on other pins if the VDD or VSS connection has resistance (1 Ohm is enough) or inductance (a few nH is enough). This complication is not present in the CDM data.

Therefore, if no other information is available, using CDM data might be pragmatic, but it is a better approach to extract the correct information using, for instance, a VFTLP system.

4.2.3 Category 2

There are no standardized tests for transient latch-up. Some tests used in the field are listed below merely as examples.

Note that for all tests, a relevant supply should be used to power up the component, as parameters such as source impedance and response time are critical.

Next, Sections 4.2.3.1 through 4.2.3.3 will give some examples of how TLU is dealt with in the industry; similar techniques and characterization methods might have merit for avoiding failures during IEC 61000-4-2 as well, though none of them are generally accepted as solving the issue of a TLU triggered by an IEC 61000-4-2 pulse.

4.2.3.1 Triggering of Supply Clamp during ESD System Level Tests on a Form-Factor Board in a Mobile Application

This example addresses a TLU trigger induced by a system level stress. A baseband IC in a 65 nm complimentary metal-oxide-semiconductor (CMOS) process latches up during an IEC 61000-4-2 ESD system level stress of the entire mobile form factor. The physical root cause for the latch-up was triggering the power clamp in one domain. Electrically, the latch-up could be detected by

increased power consumption on the particular power supply. For a complete discussion, see Technical Report TR-5.4-5 of the ESDA, which should be released by the end of 2012.
The baseband product passed the (static) latch-up test according to JEDEC JESD78D up to 150 mA of injected current at a temperature of 85 °C. In the JEDEC latch-up test, the compliance was set to 1.5 times the absolute maximum ratings (AMR) according to the JEDEC JESD78D spec. If higher compliance values are used, the transiently triggered latch-up could be reproduced by the JEDEC JESD78D stress. In Figure 17, the DC I-V characteristics of the power clamp are shown. The power clamp's holding voltage is significantly below the supply voltage, the clamp's trigger voltage, however, is above the levels tested in the LU overvoltage test. To identify the latching silicon controlled rectifier (SCR), the IC was analyzed by EMMI. As shown in Figure 18, the EMMI spot was localized over the power clamp.

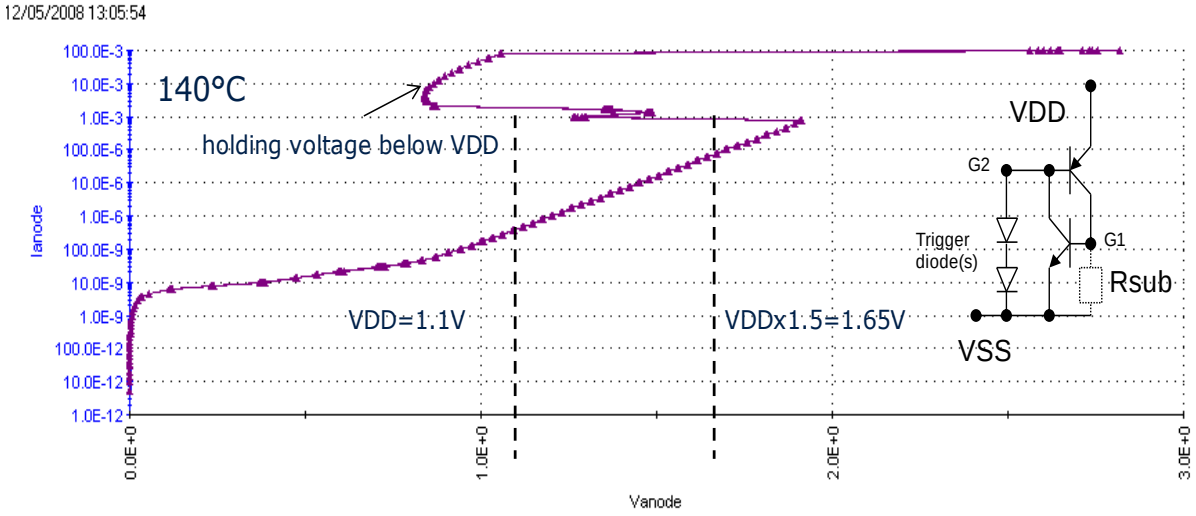


Figure 17: DC I-V characteristics of the diode triggered SCR power clamp. The clamp has the holding voltage below VDD; this posts a potential issue for LU/TLU. It is, however, not sensitive to slew rates, because it does not contain any breakdown elements or RC trigger circuitry

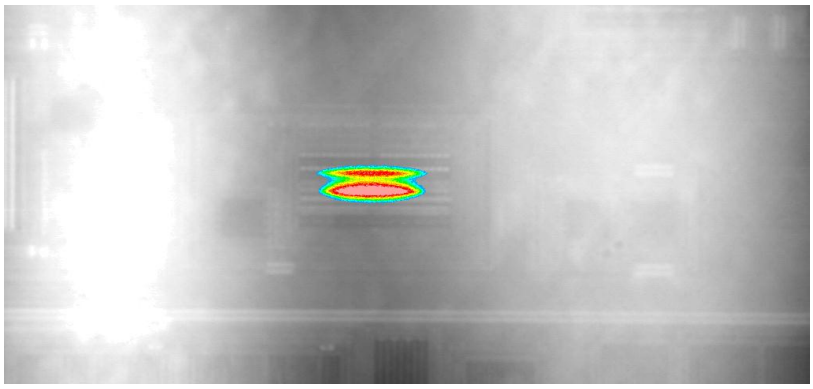


Figure 18: EMMI snapshot of the power clamp after EOS stress. The emission spot indicates that the component has latched (courtesy of TR-5.4-5)

Consequently, the latch-up phenomenon observed in that baseband product is not a "true" TLU phenomenon, because it is not dependent on the latch-up pulse slew-rate or duration. The SCR is triggered due to overvoltage and associated current injection. Obviously, a system level stress can

induce quite high current amplitudes into the IC; at least considerably higher current levels than defined in the JEDEC JESD78D qualification tests. However, using such high currents far beyond the AMR in static latch-up tests would very likely cause EOS or gate oxide damage, which of course is not the focus of latch-up testing.

Transient TLU pulses are used in this example, in order to avoid overstress failure. The parameters of the transients (rise time, pulse duration …) do not play any significant role as long as the pulse duration is short enough to avoid overstress and the current amplitude is high enough.

4.2.3.2 CDE triggering TLU

It is not surprising that fast transients, which occur during CDE or ESD system level surges according to IEC 61000-4-2, can potentially trigger latch-up.

CDE using cables with lengths of 1.5 m, 10 m, 20 m, and 40 m were applied on an IO pin of a specially designed IO test chip at 100 °C ambient temperature. Only trigger currents with negative polarity were applied and the values of the trigger currents are given in absolute numbers.

No latch-up was observed for the shortest cable. For the longer cables, increased power consumption at the voltage supply VDDP1 indicated latch-up for charging voltages between 240 V and 580 V; the corresponding waveforms are depicted in Figure 19 [9].

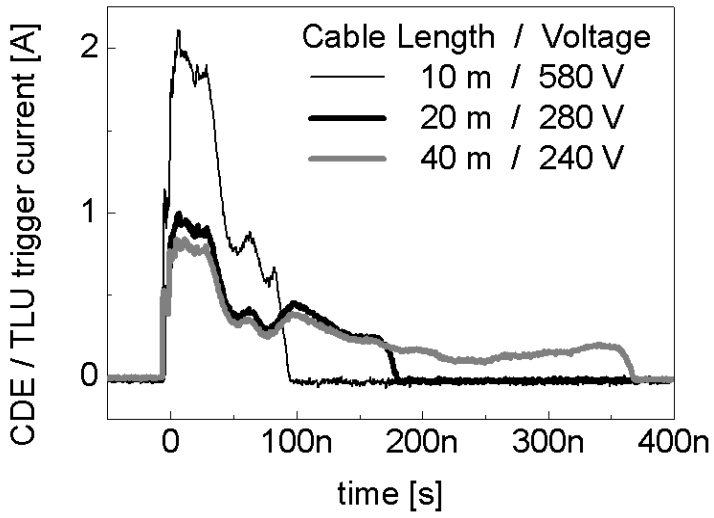


Figure 19: CDE waveform for 10 m, 20 m, and 40 m long cables after they are charged with voltages corresponding to the CDE / TLU trigger threshold of TC2_IO1 [9]

No latch-up at the second voltage supply (VDDP) could be induced by CDE. This observation is surprising because the results of other TLU tests estimate a lower threshold level at VDDP (see Figure 20). Again, crowding of the substrate current might favor the triggering of latch-up at voltage supply VDDP1.

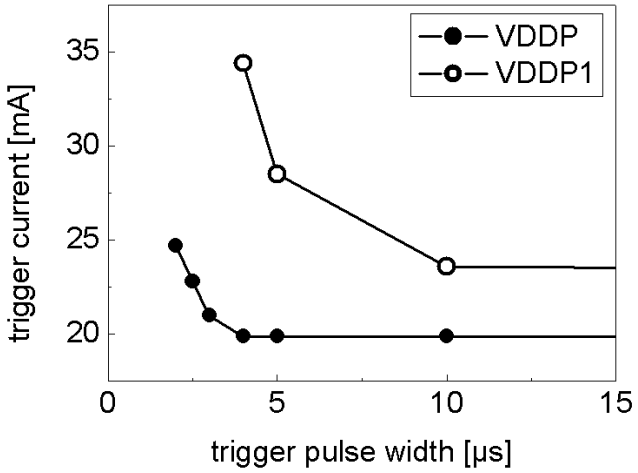


Figure 20: TLU threshold trigger current (negative polarity) of IO1 pin of TC2 versus duration of the trigger pulse (81104A, t_r = 10 ns) at 100 °C ambient temperature (courtesy of TR-5.4-5).

External latch-up can be triggered even by comparably short cables (cable length = 10 m). The CDE trigger current threshold can be two orders of magnitude higher compared to the "static" latch-up trigger level. Thus, the TLU sensitivity in terms of injected current amplitude is significantly relaxed compared to static latch-up. However, during TLU events high voltage amplitudes can appear. This may be one of the reasons why components can fail during CDE stress even if they pass JEDEC JESD78D. The CDE trigger can be well reproduced by TLP. This has to be considered carefully in upcoming standardization activities.

4.2.3.2 Transient Latch-up Tested through Capacitive Discharge

CCL (capacitive coupled latch-up, also referred to as ESD induced latch-up) is a test which is popular in the Middle East and Japan. A bipolar HV pulse is applied to an IC under powered up conditions. Though there is some merit in using this test to predict the ICs susceptibility for transient latch-up, there is some mismatch in the peak current vs. energy in the bipolar pulse versus the assumed field case. A 200 V pulse using a MM generator has a peak current of 3 A, which corresponds reasonably well with the expected peak current of the field case (though this consideration better fits Category 2), but the time duration of a bipolar stress pulse is much larger, such that applied energy is too high, which might lead to a destructive failure which is not transient latch-up related. In general, the applied voltage for the CCL test should not exceed the MM capability of the IC. In [27] it is explained that the use of such a bipolar stress is useful, but the test in this reference uses a waveform of a lower frequency (using a 20 Ohm source) than the MM stress. In [10], a comparison is made between 0 Ohm (MM) and 20 Ohm pulses for characterizing the transient latch-up susceptibility.

4.2.3 Category 3

Though many Category 3 soft failures have been solved, there are few very well documented cases showing the analysis and the solution.

In depth or trial and error methods can be used for ESD soft failure analysis. The trial and error methods usually incorporate:

- Changing the assumed current path through shielding or "ground" connections and observing changes in the system behavior. For example, the improvement of the shell to chassis connection if an ESD strike to a USB cable causes errors in a USB connection.
- Adding filters such as ferrite beads and capacitors to traces that are suspected to carry the disturbing signal to an IC. For example, if the fast changing electric field couples into the key pad of a cell phone and wakes the phone from sleep mode (as the phone mistakes the induced currents in the high impedance keypad circuitry as a user action) then adding capacitors to the traces will slow the response to a point that the charges induced by the rapidly changing E-field are insufficient to overcome the threshold voltages. Another example is adding resistor/capacitor (RC) filters, like 1 kOhm/100 pF, to a reset line to avoid unwanted responses to a narrow pulse induced by the magnetic field of an ESD event.

In depth analysis methods may utilize a more systematic approach:

- Conducting system level ESD testing such that repeatable results are achieved (avoidance of air discharge, verification whether secondary ESD occurs, usage of a sufficiently large number of pulses, test for repeatability, determination of failure threshold by increased test levels in small increments, and tests of multiple units.) [28].
- Near field susceptibility scanning to identify sensitive nets, modules and ICs which show the same failure mechanism as observed during system level testing [29].
- After sensitive nets have been identified, direct injection through small capacitors can be used to quantify the sensitivity of a net. During this injection the injected current is usually measured using a current clamp.
- Current spread scanning to try to visualize the coupling paths [30].
- Quantification of the coupling path to the net by substituting the ESD generator by a network analyzer driven ESD generator and probing the sensitive net [31].
- Numerical modeling of the system on block level to determine the current densities and transient voltages between metal parts during and ESD [32].
- Tracing the root cause from the software side by analyzing register information. [33-34].

In summary, the methodology associated with systematic and relevant characterization of components addressing category 3 fails has not yet reached the level of sophistication associated with the methodology for category 1 and 2 failures. To advance beyond the empirical trial and error approach as the standard used by many companies will require a significant development effort.

References

[1] D. Johnson, H. Gossner; "Study of System ESD Co-design of a realistic Mobile Board", Proceedings of 33rd EOS/ESD Symposium (2011), pp. 360-369

[2] G. Notermans, S. Bychikhin, D. Pogany, D. Johnsson, D. Maksimovic, "HMM–TLP correlation for system-efficient ESD design", Microelectronics Reliability, 2011

[3] zur Nieden, F.; Scheier, S.; Arndt, B.; Frei, S.: „Gefährdung von integrierten Schaltungen durch Überkopplungen zwischen Leiterbahnen auf Platinen", ESD-Forum 2011, Munich, Germany, 2011

[4] S. Poon, T. Maloney; "Shielded Cable Discharge Induces Current on Interior Signal Lines", Proc. 29th EOS/ESD Symposium (2007), pp. 311-317

[5] JEDEC Standard "IC Latch-Up Test"; JESD78D; November 2011.

[6] Ming-Dou Ker, Sheng-Fu Hsu. "Physical Mechanism and Device Simulation on Transient-Induced Latch-up in CMOS ICs Under System-Level ESD Test" IEEE Transactions on Electron Devices, vol. 52, no. 8, August 2005, pp. 1821-1831

[7] Farzan Farbiz and Elyse Rosenbaum. "Understanding Transient Latch-up Hazards and the Impact of Guard Rings", International Reliability Physics Symposium, 2010, pp. 466-473

[8] K. Domanski, B. Poltorak, S. Bargstaedt-Franke, W. Stadler, W. Bala. "Physical fundamentals of external transient latch-up and corrective actions", Microelectronics Reliability 46 (2006) pp. 689–701

[9] Brodbeck, T.; Stadler, W.; Baumann, C.; Esmark, K.; Domanski, K; "Triggering of Transient Latch-up (TLU) by System Level ESD", EOS/ESD Symposium 2010, pp. 1-10

[10] I. Morgan, C. Hatchard, M. Mahanpour, "Transient Latch-Up Using an Improved Bi-polar Trigger", Proc. 21st EOS/ESD Symposium (1999), pp. 190-202

[11] S. Bargsteadt-Franke a, W. Stadler, K. Esmark, M. Streibl, K. Domanski, H. Gieser, H. Wolf, W. Bala. "Transient latch-up: experimental analysis and device simulation", Microelectronics Reliability 45 (2005) pp. 297–304

[12] Wang, Dening; Marum, Steve; Kemper, Wolfgang; McLain, David; "System event triggered latch-up in IC chips: test issues and chip level protection design", EOS/ESD Symposium 2006, pp. 1-7

[13] D. Bonferta, H. Giesera, H. Wolfa, M. Frankb, A. Konradb, J. Schulzc, "Transient-Induced latch-up test setup for Wafer-Level and Package Level", Microelectronics Reliability 46 (2006) pp. 1629–1633

[14] R. Llido a, J. Gomez a, V. Goubier a, N. Froidevaux a, L. Dufayard a, G. Haller a, V. Pouget b, D. Lewis b. "Photoelectric Laser Stimulation applied to Latch-Up phenomenon and localization of parasitic transistors in an industrial failure analysis laboratory", Microelectronics Reliability 2011

[15] J. Quincke, "Novel Test Structures for the Investıgatıon of the Efficıency of Guard rıngs Used for IO-Latch-up Preventıon", ICMTS 1990, pp. 35-39

[16] S. Liao, C. Niou, K. Chien, A. Guo, W. Dong, C. Huang, "New Observance and Analysis of Various Guard-Ring Structures on Latch-Up Hardness by Elackside Photo Emission Image", IRPS 2003, pp. 92-98

[17] Ming-Dou Ker, Wen-Yu Lo, and Chung-Yu Wu, "New Experimental Methodology to Extract Compact Layout Rules for Latch-up Prevention in Bulk CMOS ICs", Custom Integrated Circuits, Proceedings of the IEE 1999, pp. 143-146

[18] Ming-Dou Ker, Member, IEEE, and Chung-Yu Wu, Member, IEEE, "Modeling the Positive-Feedback Regenerative Process of CMOS Latch-up by a Positive Transient Pole Method-Part I: Theoretical Derivation", IEEE Transactıons on Electron Devices, vol. 42, no. 6, June 1995, pp. 1149-1155

[19] D. Estreich, R. Dutton, "Modeling Latch-Up in CMOS Integrated Circuits", IEEE Transactıons on Computer-Aided Design of Integrated Circuits and Systems, vol. cad-ı, no, 4, October 1982, pp. 157-162

[20] Felipe Coyotl Mixcoatl, Alfonso Torres Jacome, "Latch-up prevention by using guard ring structures in a 0.8 µm bulk CMOS process", 2004

[21] B. L. Gregory and B. D. Shafer, "Latch-up in CMOS Integrated Circuits" IEEE Transactions on Nuclear Science, Vol 20, 1973, pp. 293-299

[22] Gensuke Goto, Hiromasa Takahishi and Tetsuo Nakamura, "Latch-Up Immunity Against Noise Pulses in a CMOS Double Well Structure", 1983 Electron Devices Meeting, pp. 168-171

[23] K. Domanski, M. Heer, K. Esmark, D. Pogany, W. Stadler , E. Gornik. "External (transient) Latch-up Phenomenon Investigated by Optical Mapping (TIM) Technique", EOS/ESD Symposium 2007, pp. 6A.3-1 – 6A.3-10

[24] Ming-Dou Ker, Senior Member, IEEE, and Sheng-Fu Hsu, Student Member, IEEE, "Component-Level Measurement for Transient-Induced Latch-up in CMOS ICs Under System-Level ESD Considerations", IEEE Transactions On Device And Materials Reliability, vol. 6, no. 3, September 2006, pp. 461-472

[25] Jayong Koo; Qing C,ai; Kai Wang; Maas, J.; Takahashi, T.; Martwick, A.; Pommerenke, D., "Correlation Between EUT Failure Levels and ESD Generator Parameters", IEEE Trans. EMC. Vol.50, Issue 4, Nov. 2008 pp. 794 - 801

[26] Industry Council on ESD Target Levels, "White Paper 3 System Level ESD Part I: Common Misconceptions and Recommended Basic Approaches," December 2010, at www.esda.org or JEDEC publication JEP161, "System Level ESD Part I: Common Misconceptions and Recommended Basic Approaches", www.jedec.org

[27] M. Kelly, "Developing a Transient Induced Latch-up Standard for Testing Integrated Circuits", Proc. 21st EOS/ESD Symp. (1999), pp. 178–189

[28] Xiao, J.; Pommerenke, D.; Drewniak, J. L.; Shumiya, H.; Maeshima, J.; Yamada, T.; Araki, K.;"Model of Secondary ESD for a Portable Electronic Product", IEEE Trans. EMC, Oct. 2011, pp. 1-10

[29] Muchaidze, G., Jayong Koo, Qing Cai, Tun Li, Lijun Han, Martwick, A., Kai Wang, Jin Min, Drewniak, J.L., Pommerenke, D., "Susceptibility Scanning as a Failure Analysis Tool for System-Level Electrostatic Discharge (ESD) Problems", IEEE Trans. EMC, May 2008, Vol 50, No. 2, pp. 268-276

[30] Wei Huang; Dunnihoo, J.; Pommerenke, D.; "Effects of TVS integration on system level ESD robustness.", EOS/ESD Symposium 2010, pp. 1-6

[31] Jayong Koo, Qing Cai, Muchaidze, G. Martwick, A.Kai Wang, Pommerenke, D, "Frequency-Domain Measurement Method for the Analysis of ESD Generators and Coupling", IEEE Trans. EMC, Aug. 2007, Vol. 49, No.3, pp. 504-511

[32] Liu, D.; Nandy, A.; Zhou, F.; Huang, W.; Xiao, J.; Seol, B.; Lee, J.; Fan, J.; Pommerenke, D. "Full-Wave Simulation of an Electrostatic Discharge Generator Discharging in Air-Discharge Mode Into a Product", IEEE Trans. EMC, Vol.99, 2010, pp. 28-37

[33] Maheshwari, P.; Tianqi Li; Jong-Sung Lee; Byong-Su Seol; Sedigh, S.; Pommerenke, D.; "Software-Based Analysis of the Effects of Electrostatic Discharge on Embedded Systems" 35th Annual Computer Software and Applications Conference (COMPSAC), 2011, pp. 436-441

[34] Maheshwari, Pratik; Seol, Byong-Su; Lee, Jong-Sung; Lim, Jae-Deok; Sedigh, Sahra; Pommerenke, David; "Software-Based Instrumentation for Localization of Faults Caused by Electrostatic Discharge", 13th Ins. Symposium on High-Assurance Systems Engineering (HASE), 2011, pp. 333-339

Chapter 5: Standard Model and Analytical Tool Needs To Support SEED

Patrice Besse, Freescale
Jeffery Dunnihoo, Pragma
Harald Gossner, Intel Corporation
David Johnsson, Intel Corporation
David Klein, Freescale Semiconductor
Timothy Maloney, Intel Corporation
David Pommerenke, Missouri University of Science & Technology

5.0 Introduction

In chapter 4, the SEED methodology was divided into three categories depending on the different kinds of stress a component in a system can experience beyond the normal operating parameters of the component. For that approach to be successful, component suppliers and OEMs must agree on a standard model definition that includes the fast transient, high current response of a component's IO (Category 1), the fast transient, high current response of a component's IO and the circuits connected or in proximity to it (Category 2), and finally, in order to support Category 3, the model must move beyond single IO responses and become system aware, taking into account low level transient stress due to crosstalk between traces on the board or radiated EM fields. Having such a standard model allows:

- suppliers to focus on providing a single definition, high quality model of their IC. This model must be able to accurately describe Category 1 type stress response, but should also be extensible to Category 2 and, eventually, Category 3 type stresses.
- OEMs to use analytical tools to integrate the IC IO models into their system models and carry out system level stress analysis.
- EDA vendors to have a single definition to integrate into their existing or new simulation products.

With these points in mind, this chapter describes methods for characterizing component response to system level ESD stress with the aim of creating a model of that response. Available signal integrity and functionality focused models are generally characterized only within normal operating parameters for the device. Typically these models do not accurately describe the behavior of the component when it is exposed to extreme voltages and currents over the short duration of an ESD event. We will show how correct characterization and modeling can be used to optimize new designs for ESD robustness as well as debug and understand these failures in existing designs. Also, because current modeling and simulation tools are limited, methods for examining existing full system designs are presented.

This chapter is divided into three sections. The first section introduces the standard model and component pin characterization required to support the Category 1 design approach. The next section expands the standard model to encompass the requirements of the Category 2 approach. Further discussion of the component characterization follows for the additional level of required detail. In the final section, Category 3 analysis recognizes that the nodal analysis focus of the first two sections may not fully capture the system level response to ESD stress. This section examines

what to do when software analysis proves insufficient and hardware analysis of a prototype or finished system is necessary. Category 3 analysis moves beyond nodal analysis into full 3D field solver analysis based on overall system level susceptibility to spatial E- and H-fields. The use of 3D EM scanners and antennas to determine both the susceptibility of a system to induced fields and the strength of those fields in a system are described. Finally, we describe how, in the near future, this model/system structure could be extended into the EM simulation realm by extracting a field susceptibility model from a 3D EM scan and running full-wave 3D simulations to predict not only hard failures, but perhaps difficult to analyze soft failures as well.

5.1 Component Characterization and Model Requirements to Support SEED Category 1

The level of detail required by different OEMs varies with the level of sensitivity of the components used in their systems and the system operating environment. The Category 1 standard model must provide for simulations that range from simple pass / fail analysis to full current, voltage and frequency response.

5.1.1 Standard Model Needs to Enable SEED Category 1 Level Analysis

To enable Category 1 basic nodal analysis, the standard model must:

- accurately describe the characteristic current and voltage response of each component pin to direct and indirect ESD stress, both with the component powered and unpowered.
- accurately describe voltage and current levels at which hard failures occur.
- extend from a simple pass/fail type simulation for a given pulse shape to the full pin response to the given ESD stress.

To do this, the model must contain the basic elements that describe the ESD behavior of a component. These are:

1. Description of each interface pin's inductance, resistance, and capacitance.
2. Description of the voltage and current response to each pin when exposed to ESD level stress events. This could be an equation that curve fits to the pin's behavior when tested. It could also be a set of data tables that presents the reponse of each pin to voltage, current and the frequency and duration of these stimuli. Multiple equations or tables may be necessary to describe the behavior of the pin when the component is powered, unpowered, or in a particular logic state.
3. Description of the failure criteria. This could be as simple as a pair of voltage and current values beyond which failure is expected to occur. Or, because failure is often dependent on the duration and rate of change of the ESD pulse, this might be described as points in the data table or equation surface beyond which characterization data says either an oxide will break down or the current density will exceed the pin's current handling ability and thermal runaway or metal fusing will occur.
4. Description of the behavior states each pin transitions through as it is exposed to ESD stress levels. Behavioral modeling allows the model to account for the cumulative effects of multiple stress events and other effects that a look-up table or curve fit model would be unable to provide.

5.1.1.1 Existing Model Standards that could be adapted to include the SEED Standard Model

There are many different models available in the industry, ranging from high level hardware description languages (HDLs) that describe the behavior of circuits and systems of circuits to SPICE compact models that describe the behavior of individual components such as transistors and resistors. There are also technology computer-aided design (TCAD) models, but because they are based on fundamental physics, they would not be suitable for system level modeling given presently available computers.

Traditionally, an IC designer would often use SPICE type models to simulate the continuous electrical or analog behavior of their IC. They might also use event driven HDLs to describe the logic behavior of the IC. A system designer would be most familiar with high level HDL models that describe the overall system behavior using an IO Buffer Information Specification (IBIS) or similar model to ensure electrical and signaling compatibility between the various components in their system. Relatively recent extensions of HDLs have allowed them to simulate both event driven logic behavior and continuous time analog behavior. Coupling between the two types of simulation allows digital or logic events to trigger analog events and vice versa.

The model that will best support SEED Category 1 will need to work at both a high level (pass/fail) for overall system robustness simulation and at a low level (I-V response) to allow for optimization of the system by providing detailed information which can be used to determine the necessary upstream protection and filtering components. Therefore, a successful model will need to encapsulate both high level behavioral modeling with the ability to dive into the details low level models afford. For this reason, HDL languages that provide behavioral modeling with analog and mixed signal capability should prove useful.

Behavioral modeling offers many advantages. Computing time is only a few seconds with a good convergence. Intellectual property is kept proprietary as no design architecture or description is required.

Behavioral modeling can be used to describe the transient behavior of an integrated circuit submitted to external stress such as an ESD event. It can be useful to simulate high injection phenomena on a nanosecond time scale, where limitations of existing compact models often appear. Depending on the complexity of the circuit, the model can be built to simulate the response of an entire IC when a pin is stressed with an ESD event or to describe only a part of the circuit such as the ESD protection [1].

Usually behavioral models for ESD are based on TLP measurements (100 ns). Main transient parameters are extracted from the TLP curve and reported in equations to describe the I-V response of the pin under ESD stress. Behavioral models are particularly good at modeling non-linear behaviors such as strong snapback in the case of SCR protection mechanisms. Different techniques exist to improve simulation convergence in the VHDL-AMS language [2].

Of course there are limits. Behavioral models can be particularly difficult to create if different biasing conditions exist. Resonance or dv/dt effects can also be missed.

Recently several papers have reported a good correlation between the level of robustness predicted by behavioral models and the level observed when a component was stressed with a TLP zap or a human metal model (HMM) zap using a 330 Ohm gun discharge. The correlation was validated when the models predicted the IC failure, which was due to energy overstress leading to permanent damage [3, 4]. In this case, failure criteria based on time to failure measurements (energy dissipation capability of the DUT depending on the stress duration) can be defined [5] and successfully used to predict damage after ESD system level stress. This kind of simulation can be performed with the addition of external protections and PCB models.

One option which makes this information available for current simulators is to map it to IBIS multi-lingual models. The ultimate objective is to facilitate a reference methodology for capturing and merging ESD simulations, models and parameters into industry standard signal integrity and functional simulation workflows. ESD pulse generator models can be used with “ESD ready” component models in existing simulator environments to predict overall system robustness and pinpoint potential susceptible problem areas.

There are currently three methods to support ESD modeling in common simulation environments:

1. **Use environment variable watching:** All simulators have some type of watchpoint environment variables that can be set for system-level nodes. The simulator would flag a environment variable when stress levels beyond the SOA are detected. The drawback to this method is that the system designer must manually calculate/assess what these limits actually should be at the system level. This requires extensive knowledge and background in ESD simulations and interactions, in addition to both considerable expertise in the simulator environment and full-system level functional and signal integrity simulations. Contrary to typical workflow, this requires manually assigning accurate system nodal I/V limits extracted from individual component characterizations. This places a considerable time and error-prone burden on the system designer.
2. **Virtual SPICE signals:** In this technique, a virtual circuit with nodes that are not exported to pins creates a virtual "FAIL" signal when component ESD_SOA stress limits are reached. This is supported commonly across platforms and would be supplied independently by component vendors inside their functional SPICE model. This is probably the most accurate, immediate and widely supportable option at this time. The drawback of this method is that this will require model support from the component vendors which is not commonly in place.
3. **HDL error messages:** This is a HDL abstraction of the SPICE method above where a Verilog-A or VHDL-AMS model referenced by an IBIS model provides stateful monitoring of I/V levels and "prints" an error message during simulation when ESD_SOA parameters are exceeded. Beyond what a SPICE model would provide, some stateful information could be handled in HDL about cumulative damage or stress level effects. The problem with this approach is that at present many lower-cost license and simulator packages do not incorporate analog HDL functionality.

As noted, all of these methods have limitations. The best solution will be one that is accurate and still easy to incorparate into the existing tool chain for the end user: the system designer. Looking forward, the best long term solution may be to extend the IBIS standard to include optional ESD

specific (model specification) parameters. This will involve adding appropriate ESD SOA characterization parameters as defined by workgroups and presented to IBIS for adoption. In this case, the simulation vendors could incorporate specific ESD analysis capabilities. This would reduce the burden on the system designer by automatically propagating appropriate watchpoint levels throughout the netlist at each instance of an "ESD ready" model.

Eventual implementation could be as simple as importing the ESD SOA parameters as nodal current/voltage limits for a pass/fail ESD test when a standard ESD pulse model is applied to the system. This modeling proposal will require a concerted effort from both the component vendor and system design communities to settle on the appropriate parameters and characterization methods that can then be presented to IBIS for adoption.

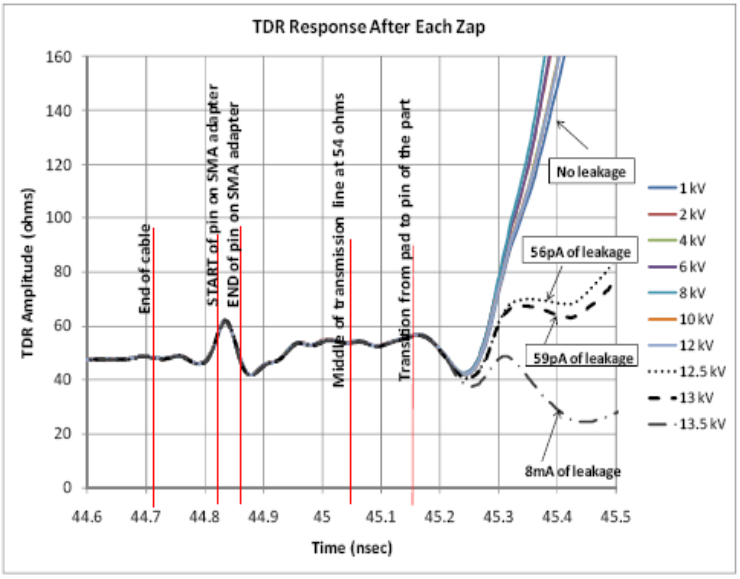
At present, there is no accepted standard system level (IEC 61000-4-2) aggressor simulation model, nor does the standard lend itself to a common model that fits all the tests that have grown out of the standard. Such a standard system level aggressor model should also be pursued as an integral part of the modelling proposal mentioned above. In the meantime, while good models should provide rational results for a range of aggressor models, vendors should carefully identify which aggressor model or model(s) are verified with their component models [6-8].

5.1.1.2 Cumulative Multi-Strike and Other Extensions

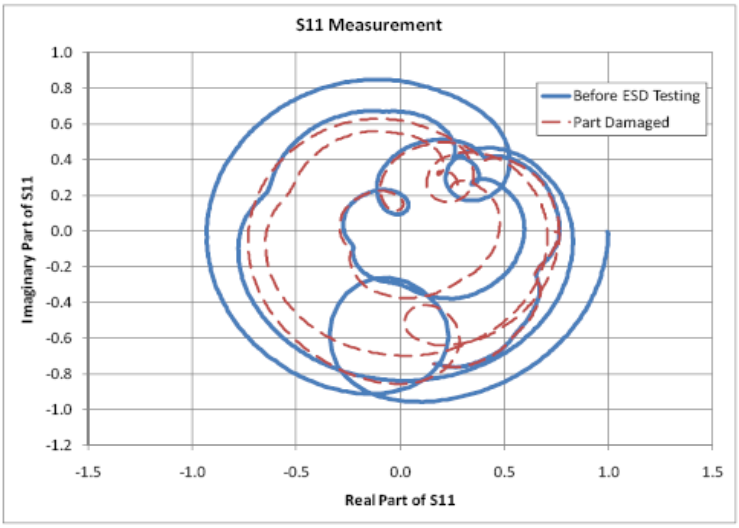
An ESD event as understood by the basic SEED methodology does not exclude dynamic failure criteria or other real-world approximations of cumulative ESD damage from subsequent ESD events. A simulation with fixed failure criteria will not address the case where a component forms filaments and maintains good leakage and clamping performance for nine strikes but fails on the tenth. Some research [1, 9, 10] has been done to model the dynamic characteristics of components as noted above, but this could be extended during the simulation to include dynamic derating of the performance and parasitic characteristics of a component to more accurately portray the SOA with respect to subsequent ESD events.

A mixed-mode model (with event driven behavioral states) could provide many important enhancements to understanding and potentially predicting accurate system susceptibility and failure modes. In the most basic usage, a state-driven model might simply encapsulate a “run-time” state where the model presents signal-integrity and functional performance, and a “clamping” model which is selected when voltages and currents enter the ESD domain. Alternately, a complete analog model of a functional buffer and clamps may cover inside and outside the run-time “SOA”. However, when the ESD SOA is exceeded in the model, the simulation advances to a “fail” state where the component becomes a short or open, for example.

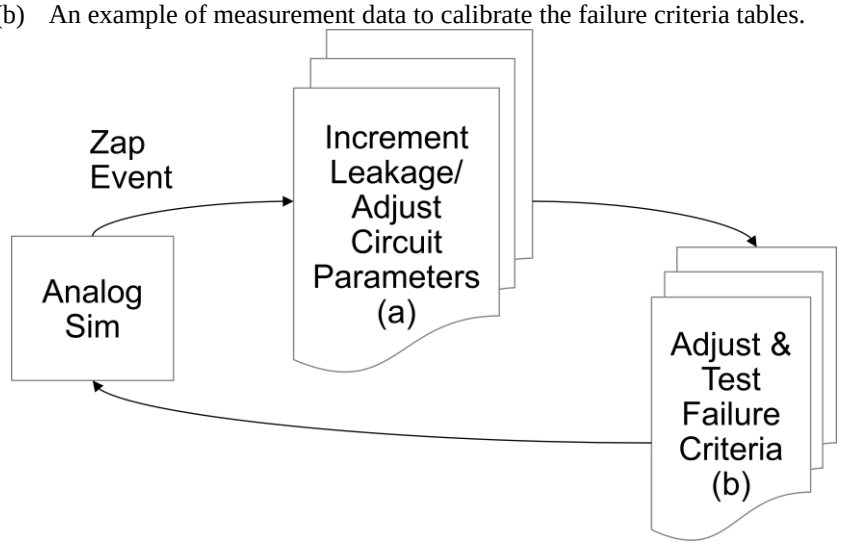
Cumulative damage and soft-failures at the system level could be simulated in more advanced models with the same approach. For cumulative damage, each strike may advance a “damage state” in the model which presents different leakage and SOA limits resulting from previously applied stresses as shown in Figure 21. For example, in the case where a TVS component is rated for 1000 strikes at 8 kV IEC and 10 strikes at 16 kV, it may be possible to model the specified limits from these datasheet parameters. It may also be possible to model them more accurately as cumulative energy dissipated and/or peak power applied, or any number of unique damage mechanisms.



(a) An example of TDR data used to create model leakage and damage tables.



(b) An example of measurement data to calibrate the failure criteria tables.



(c) Resulting mixed mode behavioral model.

Figure 21: Conceptual State Diagram of a Cumulative ESD Damage Device Mode [11]

The IBIS model container provides a potential comprehensive transport vehicle for transmitting this advanced information more accurately from the chip designer to the system developer. The market can then exploit advances in the research and adopt them within a common (optional) transport mechanism which vendors can support with minimal accuracy (basic static SOA with conservative guard-banding for multiple-strikes) or extended accuracy allowing, more aggressive ratings (with dynamic SOAs that describe a distribution of ESD robustness and susceptibility.)

5.1.2 Component Pin Characterization Description

The most widely used tool for analytical ESD characterization is TLP. A TLP is based on a transmission line which is charged to a high voltage. The line is discharged through a mechanical switch, which gives rise to a rectangle-shaped pulse. The pulse width is defined by the length of the transmission line. The rise time of the pulse depends on the spark formation speed in the switch, which is usually in the range of 100 ps. The ability to form such steep pulses at voltage levels of several kilovolts makes the TLP an ideal instrument for measuring components in the ESD regime. The approximately square-shape of the pulse allows the component to settle into a quasi-stationary state where the voltage and current over the component can be measured. The well-defined coaxial environment is also of advantage since RF metrology methods can be applied to measure the turn-on response of a component in the sub-ns regime. The most common TLP systems are discussed below and Table 3 shows the recommended parameter settings for system level characterization.

Table 3: Recommendations for a TLP system suitable for system level characterization

Pulse amplitude	At least 30 A
Rise Time	0.5 ns & 10 ns
Pulse widths	2.5 ns & 100 ns

Standard TLP

The most commonly used TLP pulse width is 100 ns since it corresponds well to an HBM discharge. A rise time of 10 ns is usually selected for the same reason. The system creates the I-V curve by averaging every applied pulse in the window at the end of the pulse when the component has settled to a quasi-stationary state and any ringing due to inductance in the connection path has decayed. The component probe setup is often not optimized for high frequencies, which makes it hard to study fast transient effects.

Very Fast TLP (VFTLP)

The term very fast TLP (VFTLP) commonly refers to a TLP system with a pulse width below 10ns and a rise time below 1 ns. A VFTLP system uses advanced RF probing methods to capture the transient turn on response of a component. Since VFTLP pulses are much shorter in duration, components can be measured to higher pulse levels without thermal destruction. This addresses other failure mechanisms relevant for the CDM regime. VFTLP is also suitable for investigating the susceptibility of a component to the first peak of an IEC 61000-4-2 pulse.

Combined TLP/VFTLP systems

Differentiation between standard TLP and VFTLP systems is only historical. Today several test systems can deliver any combination of pulse width and rise time, and with a suitable probe setup,

the transient response can be measured for both short and long pulses. This is a great advantage since only a single system is necessary to characterize both transient turn-on effects and thermal destruction.

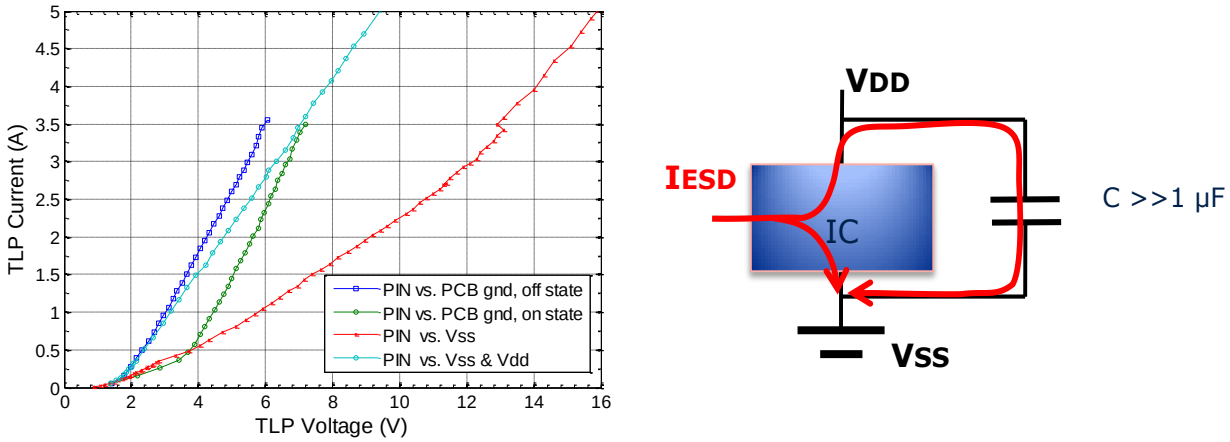
5.1.2.1 Characterization of ICs

In order to use the SEED methodology, the I-V response of the relevant IC pins exposed at the system level must be known. It is also necessary to know how much current an IC pin can handle without being damaged. Even if an IC is not specified for more than 1 kV HBM, it is inevitable that external pins will be exposed to higher stress in application. System designers often follow a trial-and-error approach, which results in designs where several pins may be exposed to currents in the range of 10 A. IC manufacturers may be reluctant to rate external pins to such high current levels, but it would be a great advantage for both the IC manufacturer and the system designers if such data would be made available.

The current robustness of an IC pin depends on the applied pulse shape, which can vary greatly depending on which pulse form is applied. The IEC 61000-4-2 pulse has a time constant around 50 ns. However, the pulse appearing at the IC usually looks very different from the IEC shape due to the impedance transformation that takes place at the external protection component. The pulse through the IC has lower amplitude, but often longer time duration. A pulse width of 100 ns TLP is a good approximation for a residual system-level pulse and easily created.

Measurement configuration

There usually are several paths for the ESD current to flow through an IC. Thus, the response of a certain pin can vary depending on how the other pins are terminated and the state of the system. An example is shown in Figure 22(a), where the I-V curve is presented for a typical system-level ESD relevant pin in different configurations. The curve “PIN vs. VSS” shows the measured I-V response between the pin and the GND pin of the same domain. However, when the IC is measured on a PCB, the curve “PIN vs. PCB GND, off state” is obtained. Note that the voltage of the pin is almost half, which would lead to higher current through the IC in a co-design configuration. The reason for the lower voltage is the parallel ESD current path through the VDD pin (Figure 22(b)). The relatively high quality (ceramic) capacitors placed between VDD and VSS have lower impedance in the ESD region. Thus the Vdd bus can be considered equipotential to ground for an ESD pulse. With the system powered on, the higher potential of the VDD bus will change the pin response. This is shown in the curve “PIN vs. PCB GND, on state”.



(a) (b)

Figure 22: a) I-V curves for a typical external pin measured in different configuration. b) Schematic figure of the current flow through an IC with second discharge path over VDD.

The previous example shows that ideally an IC should be characterized in a configuration similar to its final application. However, it is tedious work to test every pin on a product PCB, since the IC must be replaced after every destructive pulse. It is also necessary to remove external protection elements from the PCB to obtain the component response alone.

Figure 22(a) also shows the IC measured with both VSS and VDD grounded. This curve is very similar to the curve obtained with the IC mounted on a system PCB. Since this curve can be considered "worst case" for a co-design, this configuration can be used to systematically test an IC. An advantage of this configuration for parts where all the internal grounds are shorted together in the package is that the IC can be measured in a 3-pin setup, either in a socket or with needle probes touching down on the IC bumps/pins. To make such a simplification, the ESD paths of the IC must be carefully analyzed to pick the correct pins to be grounded during the test.

5.1.2.2 Characterization of External Protection Components

The external protection component is the first barrier that keeps ESD pulses away from the main IC. Its turn-on speed is crucial for achieving high system robustness against ESD. Even if a certain voltage overshoot can be tolerated, it is a good practice to use components with as fast a turn-on speed as possible. A TLP system with a rise time on the order of 0.5 ns is ideal to measure the turn-on characteristics of a TVS. To connect the package, a test board like the one presented in Figure 23 can be used. This test board incorporates a 50 Ohm micro-strip line connected on both sides with sub-miniature version A (SMA) connectors. The 1 kOhm resistor is used as a voltage divider to give a scaled voltage at the port "Pulse Sense". The resistor can also be omitted to directly measure the residual voltage arriving at the pulse sense port. In this case pulse withstanding attenuators must be placed in series with the oscilloscope input to protect it from damage.

An alternative setup is presented in Figure 24. This figure shows a TVS contacted with Cascade RF probes in a Kelvin configuration: one probe is used to deliver the pulse and the second to sense the voltage. This setup achieves the best transient resolution of the measurement, but needs expensive equipment such as a probe station with micro-positioners and RF probes. An example of voltage waveforms captured with the setup as shown in Figure 24 is shown in Figure 25.

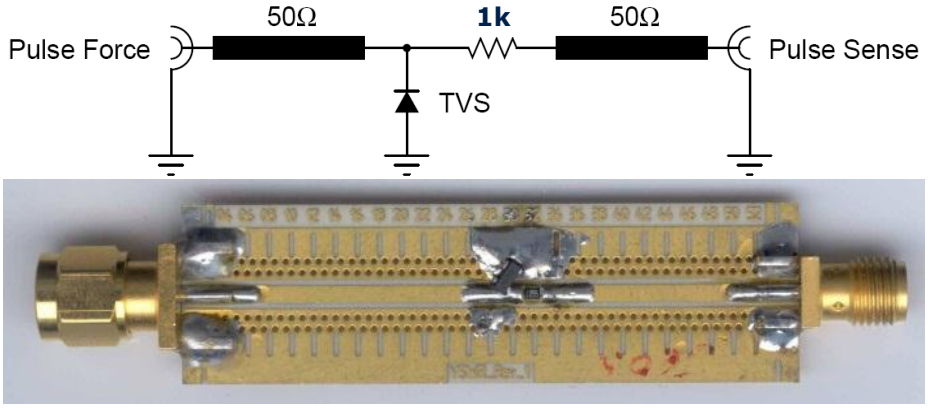


Figure 23: Measurement configuration with evaluation board

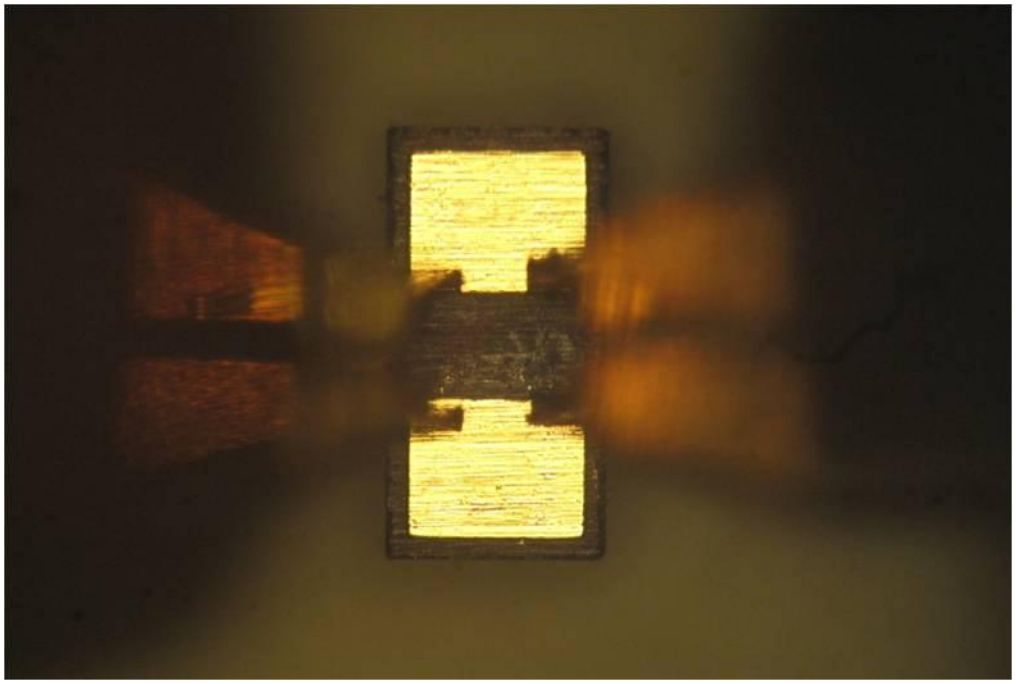


Figure 24: Measurement configuration with RF probes

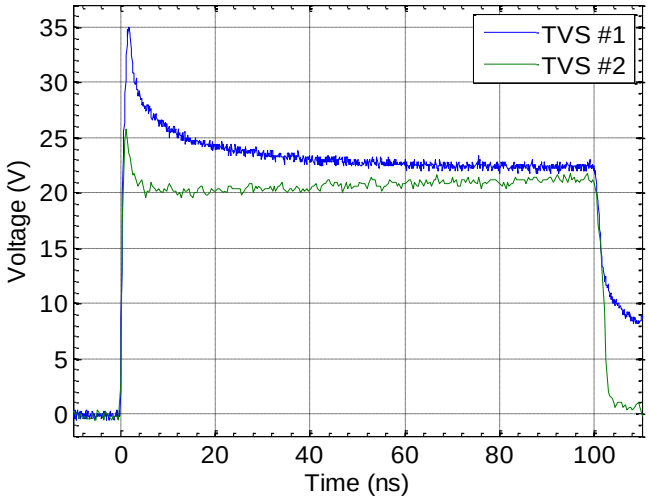


Figure 25: Example of voltage waveforms from two TVS diodes with different turn-on time. The TLP pulse has current level of 10 A and a rise time of 0.6 ns. The waveform with large overshoot is the response of a low capacitance diode. This overshoot is caused by the diode's strong conductivity modulation.

5.2 Component Characterization and Model Requirements to Support SEED Category 2

Characterizing and modeling a pin of a component is relatively straightforward when all the circuitry that can be considered connected to that pin is not dependent on the state or mode of operation of the component. Examples of these sorts of IOs are general purpose input/outputs (GPIOs) and serializer/deserializer (SERDES) interfaces. However, there are pins where the functionality and exposure of internal circuits are dependent on the system state or mode of operation. An example is a multifunctional analog pin which exposes different internal circuits to the pin depending on the mode of the component. For successful characterization and subsequent modeling of these pins, extensive testing of the IO may be necessary to determine the most susceptible (worst case) mode of operation for that specific pin. As a result, while the Category 1 models could be lumped by type, to successfully support Category 2, each pin may need to be separately modeled for its response to low energy pulsing. It is of interest to determine the pulse shape that leads to either physical damage due to latch-up or functional upset due to transient latch-up caused by injection of current into the substrate.

5.2.1 Standard Model for Category 2 Stress

Changes necessary to the standard model in order to accommodate Category 2 type stress are fairly minimal. A behavioral model that is able to model accumulated stress damage and/or accelerated triggering due to very fast edge rates can also accommodate the descriptions of pulse shapes (rise and fall time, duration, amplitude, etc.) that can lead to latch-up or system upset. The larger problem is characterizing the component to determine not only the SOA of the pin, but also to ensure that the pin's mode of operation during characterization is indeed the worst case for low pulse induced hard or soft failure.

5.2.2 Category 2 Component Pin Susceptibility Characterization

The immunity of IOs against injection of substrate current is typically probed by standard JESD78 latch-up qualification of ICs. The standard requires an injection level of 100 mA. The

pulse applied ranges in the 10 ms region. While this is a useful basis for assessing the general robustness of the IC, it might not be sufficient if short pulses of up to Ampere amplitude occur during a system level ESD event. Simply increasing the current level is usually not appropriate as 1) other failure mechanisms might be triggered due to thermal overheating and 2) rise time dependent mechanisms are neglected. Here transient latch-up testing based TLP can offer an appropriate way of characterization.

The TLP testing requirements are similar to those used in Section 5.1.2 with the following changes:

- Testing should be done under powered conditions, having realistic on board power decoupling for achieving VI curves relevant to system level design.
- Damage parameters, such as increased leakage, need to be monitored.

These modifications are necessary to detect hard failures. To characterize soft failures, further work is necessary:

- A significantly more complex test setup is needed, as peripheral ICs may be required to operate the DUT. Additional software may be necessary to cycle each pin through its possible operating modes to determine the worst case mode during testing. Also, additional components and software may necessary to detect operational changes.
- For meaningful soft failure characterization, the TLP pulse width of the injected noise should be varied from ns to µs. Such testing can be performed automatically by injecting pulses from a transmission line pulser through a small value capacitor or a high impedance resistor. An automatic scanning system can position the injection probe from pin to pin while varying the pulse strength and shape and observing the functional behavior of the IC. In special cases, narrow, possibly bipolar pulses need to be considered.

The characterization is applicable for any system external or internal IO. Supply pins are excluded. Due to the ambiguity of some supply pins, for instance pins attached to internally generated voltage, such pins should be characterized like IO pins if substrate current injection can occur through forward biased junctions attached to this pin.

5.3 System Characterization and Model Requirements to Support SEED Category 3

The modeling and characterization up till now have focused on how pins of components react to direct or induced stress. While this is very important to understand and model, the environment in which the component will be placed is also important in determining whether that component will be susceptible to damage in that system. For example, a component with low damage thresholds may be successfully used in a system where the surrounding components, PCB design and enclosure or case all cooperate to shield it from damage. At the same time, a component with a high damage threshold can easily be destroyed if it is exposed during a system level ESD event to stress beyond its SOA. For these reasons, characterization and modeling of the system are necessary.

An appropriate characterization method is not yet defined and poses a challenging task as such an approach must work for a wide range of systems. One option is to apply TLP pulses to modules,

traces, and system ports, and couple the resulting transient EM field into various parts of the system. This can probe the susceptibility of the system. Another option is to map system susceptibility by injecting noise from an EM scanning head. These options will be discussed in detail below.

Ideally, modeling and simulation of system response during a ESD strike would be carried out using full wave tools and models. However, full wave simulation is not possible at present because to model most systems in detail will result in too many variables and unknowns to be practical. However, one can model a system using a full wave block level approach. In this approach, the main metallic parts, like the enclosure and batteries or main cable connections, are modeled while the details of the PCB and components mounted on it are ignored. Excitation by an ESD generator can be included in the model. This model will provide the current densities induced on PCBs, connecting cables and the chassis. Further, it will provide an estimate of the field strengths inside the system and the current paths. This information can be used to estimate the risk of direct coupling to ICs and used as stimulus for further, more detailed simulations which might determine the coupling into a single layer flex circuit relative to a dual layer flex circuit.

At this point, let's review the tools presently available for ESD analysis [12]:

TLP for I-V characterization:

A variety of TLP concepts, such as direct current and voltage measurements exist for the characterization of the transient I-V curve of components. These can be IOs or power pins on an IC. TLP can also be used to measure the non-linearity of capacitors and ferrite beads in addition to the breakdown limits of resistors and capacitors

TLP for susceptibility scanning: [13]

In a similar fashion, a TLP can be used to couple to modules, traces and pins through the transient field. The TLP may need up to 8 kV of charge voltage to provide sufficient field strength if small probes are used. Typical rise times are < 500 ps. The TLP is coupled to the circuit using probes magnetic field probes ranging from 50 mm to 0.5 mm or similar electric field probes. These probes induce currents (E-field) or induce voltages (H-field). The induced pulses follow the time derivative of the TLP rising and falling edge, thus, they are usually less than 2 ns wide. This is not atypical for system level ESD signals that are indirectly coupled onto traces, such as at board to board connectors. Field coupled noise can be directly injected onto a trace using a small (1 pF) capacitor to connect the TLP to the trace. In this case the injected current can be measured, (for example, with a small current transducer such as one from the Tektronix CT-series). In order to directly inject current onto a trace, the scanning system should be equipped with a probe that contains either a small capacitor (such as 1 pF) or a higher value resistor (such as 1 kOhm). A probe so equipped allows connection of the TLP output to the trace. The displacement current from the local ground of the probe to the ground of the PCB is the high frequency component of the return current. The low frequency component of the return current flows through a wire connection to the PCB. Now the system can touch the probe to different nets and increase the injected pulse until an error is observed. A record should be kept of the current at which this error occurs and the observed failure phenomenon.

Susceptibility scanning:

In susceptibility scanning, a probe is usually moved automatically from position to position and noise is coupled to the traces, modules or ICs while observing the system response. At each location the soft-failure threshold is detected creating a map of the susceptibility [13].

In the remainder of this section, system level characterization and analysis will be discussed, starting with the basics of measuring crosstalk on a PCB board. Next, the discussion will briefly introduce and describe a way to observe the radiated fields inside a system. This is followed by a brief explanation of how these methods, along with susceptibility scanning, introduced in Chapter 2, can be used to debug a system. Finally, present short-comings and future directions for both modeling systems and software are discussed.

5.3.1 Investigation of PCB Crosstalk

Crosstalk between PCB lines can be investigated by TLP or IEC gun stress of test boards with aggressor and victim lines in worst case arrangement such as long parallel lines of narrowly spaced distance. An example schematic and test board is shown in Figure 26. This type of investigation is shown for a typical automotive board [14]. The induced energy and the waveform at the victim line strongly depends on the matching of the impedance and can be modified by serial resistance and shunt elements like TVS diodes and IC IO protection. All this needs to be considered when setting up the test. Recent simulations have shown that an 8 kV IEC discharge to a controller area network (CAN) line leads to significant peak currents of several amps in a neighboring line attached to a typical microcontroller IO [15]. However, due to the very short length (< 5 ns) of the induced pulse, the energy coupled to the victim line is small compared to a 1 kV HBM pulse. Thus, thermal damage is very unlikely, but CDM type damage as well as transient latch-up can be failure mechanisms of relevance.

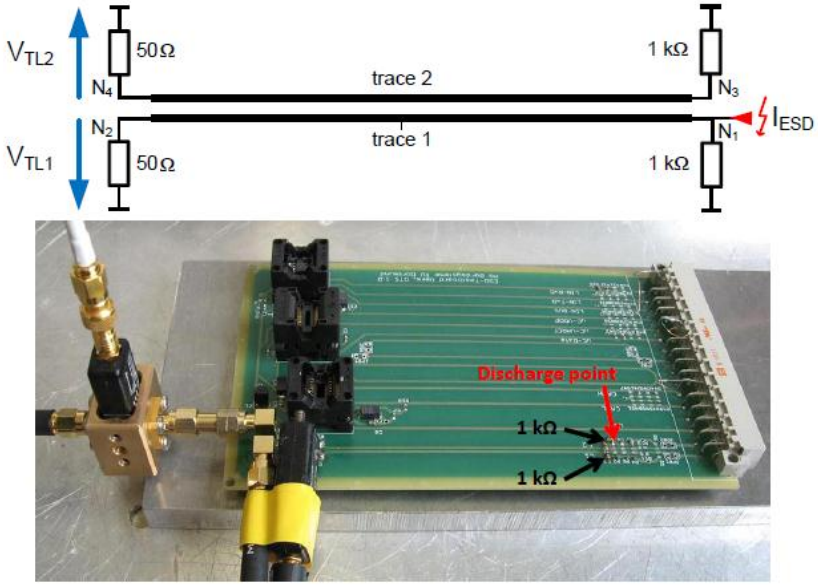


Figure 26: Crosstalk experiment for an automotive PCB [14]

5.3.2 Description of a Method for Measuring Radiated Fields inside a System Case

As discussed in Chapter 2, the concept of signal upset or soft failure refers to the kind of system crash due to signal integrity problems that can occur when a chassis is ESD pulsed according to the IEC spec. Most often this is due to electric or magnetic (E or H) fields injected into the system, despite chassis grounding efforts. Pulsed fields can be picked up by board wiring, loops, and other structures (such as heat sinks) inside the chassis, influencing signal integrity.

While the EM scanner, discussed above, examines the impact of local fields on component and system functionality, the actual IEC test or ESD event will inject fields globally into the chassis and influence all components at once. This is not an easy situation to analyze, so it is natural to want to find local sensitivities to local fields with the EM scanner. As a complement to the EM scanner, it is also useful to know the overall level and time-dependent behavior of field injection into the chassis. This is because the actual injected fields during ESD will usually not be localized, though it is these injected fields that produce many failures. A measure of the magnitude and time dependence of the internal chassis E and H fields could reveal whether field injection is high, low, or "reasonable" for the product. EM scanner results using local fields should be more meaningful in light of such measurements of global field injection.

If care is taken, internal field detection is possible using various methods of installing a transmission line and readout connections into the product [16, 17]. Micro-strip lines could be built into the PCB, but could also be retrofitted onto the chassis of a completed product. A demonstration setup showing these principles is shown in Figure 27.

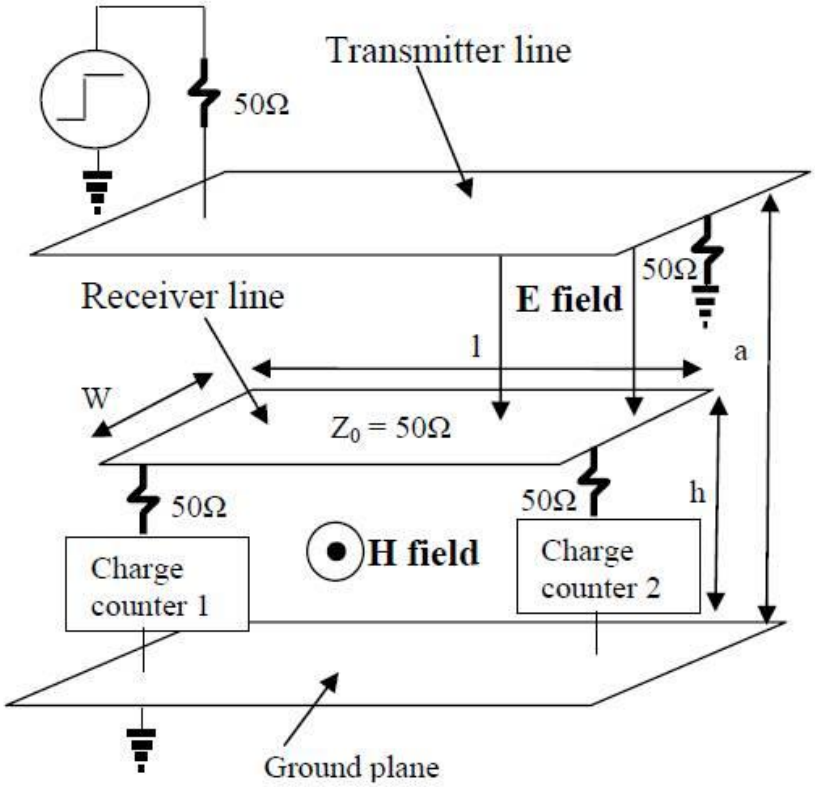


Figure 27: Transient electric (*E*) and magnetic (*H*) fields as described in [16]. Two transmission lines with characteristic impedance of 50 Ω are used, one as the receiver (middle line) and the other as a transmitter (top line).

Thus a micro-strip or similar line on a board can be terminated with 50 Ohms at both ends, and connected on one or both sides in order to read the fields (or, more accurately, the field derivatives) as described in [16, 17]. E-field and H-field strength on a given segment can be distinguished by noting the sum and difference of the signals on the two "charge counter" outputs. This kind of detector senses the time derivative of the field and the principles are well covered in review articles, for example [18].

If, as often happens, the product of interest is complete and there is no opportunity to design field detectors into the product from scratch, one can consider installing a micro-strip-like transmission line on the inside panel of the chassis. If space allows, a nearly ideal method is to use common 300 Ohm "twin lead" transmission line with 1 mm wires separated by 7 mm and embedded in plastic; this is familiar TV antenna wire. A cross-section is shown in Figure 28.

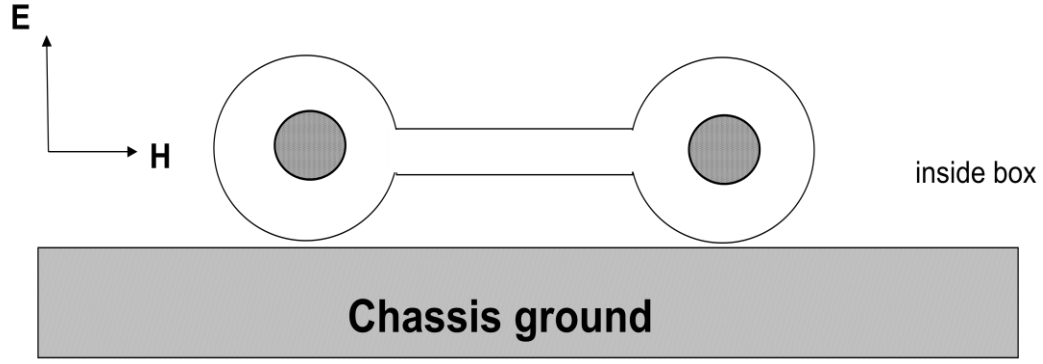


Figure 28: Cross section of twin lead wire (1 mm wires separated by 7 mm, embedded in plastic and sitting about 1 mm off the metal ground plane) mounted inside a chassis for use as an E-H field detector as in Figure 27.

Each of the two single wire lines above the ground plane (i.e., mirror plane) is equivalent to an almost perfect 100 Ohm parallel-wire line, so the two in parallel make a good 50 Ohm line with respect to the ground plane. Figure 29 shows a top view of such a detector wired to BNC connectors from the inside of a chassis. This arrangement has been shown to work very well as a field detector, and is briefly discussed in [16].

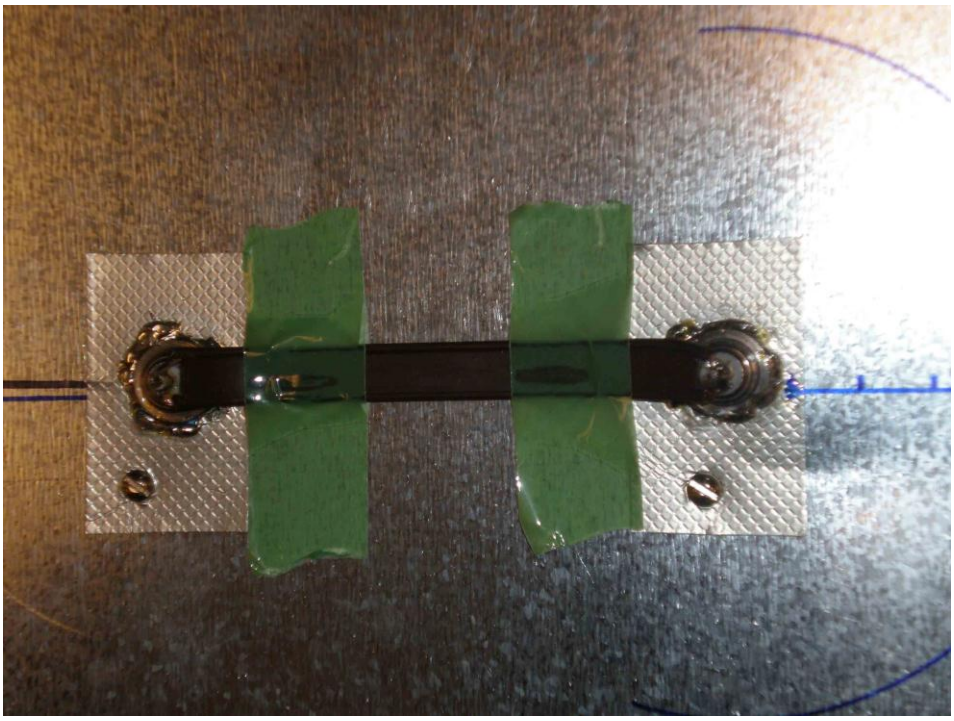


Figure 29: Top view of twin lead 50 Ohm T-line field detector, wired to BNC panel mounts.

An example of the use of this field detector follows. A new personal computer (PC) reference motherboard was installed into a standard oversize metal PC chassis but promptly failed at an unexpectedly low IEC ESD voltage when pulsed externally. The twin lead field detector was installed at a convenient place in the middle of the chassis as shown in Figure 29 and signals read out to 50 Ohm scope inputs. As expected, E and H field derivatives (determined through the sum and difference of the channels) were about the same in this location. But a fast Fourier transform (FFT) of the + and – 6 kV induced waveform yielded an interesting feature -- a sharply peaked resonance at 537 MHz (points were 50 MHz apart so the nearest were 488 and 588 MHz, both over 50% of the strength observed at 537 MHz). This box resonance just happened to be close to the 2nd harmonic of one of the IO clock frequencies (266 MHz). Apparently, the interior fields injected by the IEC pulser drove the clock transition board signal lines in the wrong direction every other cycle for as long as the pulse lasted. This sort of weakness would be hard to pick up with the EM scanner, as the chassis has to be opened and the local signal is usually a pulse. The field detector thus complements other methods of determining system ESD failure by serving as an in situ detector of exactly the kind of induced signals that could cause system upset.

In addition to the twin lead detector, it is clear that other single conductor or parallel wire schemes above a ground plane can be arranged to interface with convenient 50 Ohm outputs. For example, SMA connectors can be used for a more compact fit into a tight chassis. Today's products are a little tighter than yesterday's PC boxes, but lines made with copper tape on polyethylene tape are very compact and just need a carefully built connector interface.

5.3.3 Explanation of how these Methods can be used to Empirically Debug a System

Faced with the difficulty of a system failing a system level test, a variety of methods are suggested to identify the root cause of the failure. These methods approach the problem from three sides: system level testing, software, and near field susceptibility scanning. Please note that this list of methods is not exhaustive, other methods that are different or better may be available.

5.3.3.1 System Level Testing

System level testing cannot be reproduced well, yet measurements can be taken to obtain the most reliable information. A short list of considerations follows:

- Measure the discharge current during system level testing (such as in the ESD generator ground strap using an F-65 current clamp or similar) to test if secondary ESD has occurred. Secondary ESD will show up as a second pulse delayed by nanoseconds to microseconds after the first pulse and happens if a non grounded piece of metal is charged by the ESD causing a spark inside the product. All two-wire components are in danger of having secondary ESD. The secondary gap discharge can have a much higher current peak value and shorter rise time than the primary ESD which caused the secondary ESD. This, and the fact that secondary ESDs are often very close to the electronics of the product, emphasizes the need for controlling secondary ESDs [19].
- Test for threshold not for limits. One should not only determine if the product passes at 2 kV and fails at 4 kV, but determine the threshold of failure and its repeatability
- Apply a sufficient number of pulses. It is recommended to use a few hundred pulses in contact mode at each test point using 10 pulses a second. Of course, this recommendation may not be suitable for each product, as the standard assumes that the product can return to its baseline condition after each discharge. The baseline condition relates both to the

removal of charge and to a baseline software status in case the ESD has triggered a recovery or a self correcting cyclic redundancy check (CRC) error.

- Observe the nature of the failure and report carefully (an example of careful reporting; "striping observed in the system display and then the display turns white").
- To test if a system is sensitive to the initial pulse of the ESD generator in contact mode or to the slower discharge of the RC network, replace the ground strap with a resistive wire having around 10 kOhm resistance. This way a charge return is still possible, however, the second pulse will have a very small magnitude. Of course, this only works with battery powered ESD generators.
- It is known that soft failures are often dependent on the ESD generator used [20], as each ESD generator will create a different spectral composition of its transient fields, especially at greater than 300 MHz. It is impossible to predict which test point will react more sensitively to which ESD generator, and it is usually not possible to identify the most severe ESD generator in general, as soft failures also depend on the spectral sensitivity of the DUT which varies at each test point. However, using two different ESD generators in contact mode might give an indication of the frequency range that could cause the ESD soft failure. If both results differ greatly (> 1.5x) then it is more likely that the soft failure is caused by the high frequency content of the ESD generator's current and transient fields, as ESD generators differ more in the high frequency range.

5.3.3.2 Software

Software [21, 22] can be a great tool for identifying the root cause. However, this usually requires access to the firmware and having a firmware engineer working in close cooperation with the test labs. Internal register information often documents IO failures very well. Further, bus analyzers can provide an insight into IO related errors (provided the bus analyzer is robust). If firmware is written well, it will provide clues about unexpected events by allowing access to internal registers or a bus analyzer if one is present; if it is written badly, it will just hang up or reset without reporting. In most cases, one will need to have firmware design guidelines that encourage the firmware designers to include reporting methods that can identify the root cause of ESD soft failures.

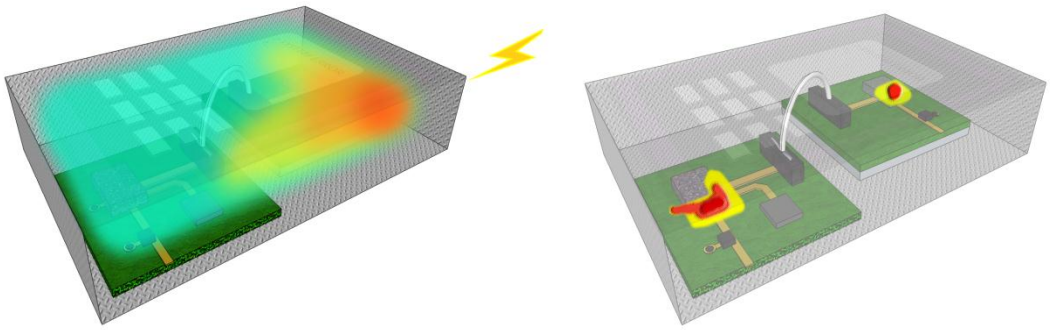
5.3.3.3 ESD Near Field Scanning

As mentioned in other parts of this white paper, ESD near field scanning injects voltages and currents into the system locally using field coupling or direct injection. If the board is scanned while observing for soft failures, one can identify the sensitive regions, nets, and ICs using near field scanning. Once those regions are identified, re-routing, filtering or software changes can be used to increase the system's robustness.

5.3.4 Software and Hardware Tool Limitations and Future Directions

The SEED methodology applies the nodal simulation concept of SOA current and voltage limits to an idealized circuit topology. In the future it could be expanded to address E and H field susceptibility limits through a full wave system simulation of an ESD strike. There are immediate computational and analytical limitations to this extension, just as there are limits to the utility and accuracy of the nodal analysis methods.

There are obvious directions in which the SEED methodology concepts could be extended. Full wave simulation of ESD pulse energy applied to the system level enclosure (Figure 30a) extends the nodal counterpart of HMM ESD circuit simulation models. 3D characterization with the susceptibility scanning methods (Figure 30b) described in Chapter 2 would be analogous to the TLP nodal characterization of components.



a) Stress applied to a system enclosure showing the qualitative E-field of the discharge

b) Susceptibility scanning with the color gradient showing increased levels of susceptibility as the color aproaches red

Figure 30: Examples of extensions to the SEED methodology

Overlaying these representations and using the susceptibility scans as a field-induced failure criteria mask against the expected field distribution of a given strike could form the basis of a complete virtual 3D component-to-system analysis before the first prototype is assembled. For example, in the simple representation of Figures 30a and 30b, two susceptibility "hotspots" are analyzed. In this particular case, shown in Figure 31, the fields induced affect the component on the right (red) and do not upset the component on the left (blue). Remedial design methods described in Chapter 3 can be carefully applied to mitigate this condition, minimizing the cost of the preventative measures as well as potentially cutting an entire prototype iteration from the design cycle. In this manner it may be possible to fully anticipate both hard and soft failures in simulation, as long as many of the practical and analytical limitations are overcome, such as the difficulty of creating a "component level" susceptibility map on an appropriate vendor evaluation board which is meaningful when integrated into an arbitrary system enclosure.

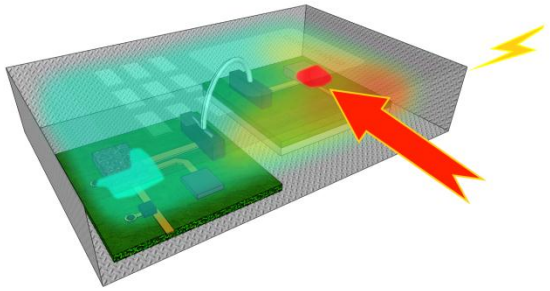


Figure 31: An example of how overlaying full wave simulation and susceptibility scanning can highlight a problem spot

At the moment, this type of analysis is beyond the capabilities of most ESD research, not to mention actual system designers. While the choice of an IBIS container can provide a platform for future expansion, the industry would welcome advanced research which can suggest an equivalent common platform for System Efficient 3D ESD Design [23].

Tools which are presently not available but within reach in the next 5 years are:

- Complete IC characterization and qualification methodologies for modules and ICs. While many sub-steps are available, there is no comprehensive method to completely characterize ICs and modules for ESD soft-failure robustness.
- Rule checker for enclosures. ESD soft failure and damage countermeasures depend on shielding, or on guiding the discharge current so that the current and associated fields do not cause unacceptable coupling. While full wave simulation can determine the current paths and fields, it is still a rather complicated method and requires very many model verification runs (we estimate that 90% of all full wave simulations are performed to verify model assumptions or simplifications). A rule checking tool that is able to import mechanical geometry files and estimate currents to flag weaknesses would reduce or eliminate the need for a full wave simulation.
- Rule checker for PCB for susceptibility. Knowing the sensitivity of the IC pins and using a matrix that connects the sensitivity of the more sensative pins with the likelihood of noise coupling (from an external IO, board to board connecting traces, long on board traces, and short on board traces) it should be possible to estimate the overall susceptibility of the PCB to coupling upset. Additional information can be extracted from the general enclosure structure and from the partitioning in different PCBs and their connections. Existing tools can extract electromagnetic PCB characteristics so that models can be created that include conducted coupling and estimated field coupling. The later might require a data base that estimates the field to net coupling by the field confinement of the structure (for example, a single layer flex has a very low field confinement). The needed field strength information can be taken from a full wave simulation at a highly simplified level or by the enclosure rule checker mentioned above. At best this will estimate the sensitivity and at least it can flag risky design choices.
- Software based analysis. It is often difficult to determine the root cause of ESD soft failures without information from the inside of the IC. This inside information can be obtained through software by monitoring things like register values and errors on internal buses.
- Simulation suite including standardized models.

5.4 Conclusion

In this chapter, we presented several methods for characterizing components and proposed models to support the SEED methodology. Using presently available models and simulation tools, ESD behavioral models can be built and simulation of components can be carried out to debug hard failures (Category 1) of components in a system and to optimize a system under design.

Next, we investigated extending these models to cover the much harder to find and correct collateral damage and soft failure or system upsets often found in Category 2.

For both categories, TLP is suggested as a powerful tool for characterization of IC pins and PCB discrete elements like TVS diodes or ferrites.

Finally, we addressed Category 3. We recognized that the present simulation tools use primarily nodal type analysis and any system is much more complex. 3D system models were discussed that would allow modeling of complex coupling due to H and E fields present in real designs. These involve using scanners to map susceptibility of components in the system. In closing, we gave ideas for future tools and models that could be used to simulate and predict system behavior from proposed board design and component selection.

References

[1] Weiying Li, Yu Tian, Linpeng Wei, Chai Gill, Weil Mao, Chuanzheng Wang, "A Scalable Verilog-A Modeling Method for ESD Protection Device", 2010 EOS/ESD Symposium, pp. 1-10

[2] Patrice Besse, Fréderic Lafon, Nicolas Monnereau, Fabrice Caignet, Jean-Philippe Laine, Alain Salles, Sophie Rigour, Marise Bafleur, Nicolas Nolhier , David Trémouilles, "ESD system level characterization and modeling methods applied to a LIN transceiver", 2011 EOS/ESD Symposium, pp. 329-337

[3] T. Smedes, J. van Zwol, G. de Raad, T. Brodbeck, H. Wolf, "Relations between system level ESD and (vf) TLP", EOS/ESD Symposium 2006. pp. 136-143

[4] Patrice Besse, Jean-Philippe laine, Alain Salles, Mike Baird, "Correlation Between System Level and TLP tests Applied to Stand-alone ESD Protections and Commercial products", 2010 EOS/ESD Symposium, pp. 151-156

[5] Yiqun Cao, Ulrich Glaser, Joost Willemen, Filippo Magrini, Michael Mayerhofer, Stephan Frei, Matthias Stecher, "ESD Simulation with Wunsch-Bell based Behavior Modeling Methodology", 2011 EOS/ESD Symposium, pp. 187-195

[6] K.Wang et al., "Numerical modeling of electrostatic discharge generators," in IEEE Trans. Electromagnetic Compatibility, vol. 45, no. 2, pp. 258- 271, May 2003

[7] S. Caniggia and F. Maradei, "Circuit and Numerical Modeling of Electrostatic Discharge Generators," IEEE Trans. Ind. Appl., vol. 42, no. 6, pp. 1350-1357, Nov. 2006

[8] R. Mertens et al., "A Flexible Simulation Model for System Level ESD Stresses with Application to ESD Design and Troubleshooting," in Proceedings of EOS/ESD Symposium, 2012, pp. 1-6

[9] N. Monnereau; F. Caignet; N. Nolhier; D. Trémouilles, "Investingating the probability of susceptibility failure within ESD system level consideration", EOS/ESD Symposium 2011, September 11-16, 2011, pp. 1-6.

[10] N. Monnereau; F. Caignet; N. Nolhier; D. Trémouilles; M. Bafleur, "Behavioral-modeling methodology to predict electrostatic-discharge susceptibility failures at system level: an IBIS improvement", Electromagnetic Compatibility (EMC) Europe, York, Uk, September 26-30, 2011, pp. 457-463.

[11] K. Muhonen, J. Dunnihoo, E. Grund, N. Peachey, A. Brankov, "Failure Detection with HMM Waveforms", EOS/ESD Symposium 2009, 5B.3, pp. 1-9.

[12] Jiang Xiao, D. Pommerenke, Fan Zhou, J. L.Drewniak, H. Shumiya, T. Yamada, K. Araki, "Model for ESD LCD upset of a portable product", 2010 IEEE International Symposium on Electromagnetic Compatability (EMC) , pp. 354-358

[13] Muchaidze, G., Jayong Koo, Qing Cai, Tun Li, Lijun Han, Martwick, A., Kai Wang, Jin Min, Drewniak, J.L., Pommerenke, D., "Susceptibility Scanning as a Failure Analysis Tool for System-Level Electrostatic Discharge (ESD) Problems", IEEE Trans. EMC, May 2008, Vol 50, No. 2, pp. 268-276

[14] zur Nieden, F.; Scheier, S.; Arndt, B.; Frei, S.: "*Gefährdung von integrierten Schaltungen durch Überkopplungen zwischen Leiterbahnen auf Platinen"*, ESD-Forum 2011, Munich, Germany, 2011

[15] zur Nieden, F; private communication

[16] T. W. Chen, T. J. Maloney, and B. Chou, "Detecting E and H Fields with Microstrip Transmission Lines", 2008 EMC Symposium, August 2008, pp. 1-6

[17] T. J. Maloney, A. Martwick, K. Wang, "Measuring Electric and Magnetic Field", US Patent application, filed Aug. 30, 2007. Issued as US Patent 7,750,629, July 6, 2010.

[18] C. E. Baum, E. L. Breen, J. C. Giles, J. O'Neill, and G. D. Sower, "Sensors for Electromagnetic Pulse Measurements Both Inside and Away from Nuclear Source Regions", IEEE Trans. Electromagnetic Compatibility, Vol. EMC-20, No. 1, pp. 22-35, February 1978.

[19] Xiao, J.; Pommerenke, D.; Drewniak, J. L.; Shumiya, H.; Maeshima, J.; Yamada, T.; Araki, K.; , "Model of Secondary ESD for a Portable Electronic Product," Electromagnetic Compatibility, IEEE Transactions on , 2011, pp.1-10

[20] Jayong Koo; Qing C,ai; Kai Wang; Maas, J.; Takahashi, T.; Martwick, A.; Pommerenke, D., "Correlation Between EUT Failure Levels and ESD Generator Parameters", IEEE Trans. EMC. Vol.50, Issue 4, Nov. 2008 Page(s):794 – 801

[21] Maheshwari, P.; Tianqi Li; Jong-Sung Lee; Byong-Su Seol; Sedigh, S.; Pommerenke, D.; , "Software-Based Analysis of the Effects of Electrostatic Discharge on Embedded Systems,", 2011 IEEE 35th Annual Computer Software and Applications Conference (COMPSAC), pp.436-441, 18-22 July 2011

[22] Maheshwari, P.; Byong-Su Seol; Jong-Sung Lee; Jae-Deok Lim; Sedigh, S.; Pommerenke, D.; , "Software-Based Instrumentation for Localization of Faults Caused by Electrostatic Discharge,", 2011 IEEE 13th International Symposium on High-Assurance Systems Engineering (HASE), pp.333-339, 10-12 Nov. 2011

[23] Liu, Dazhao; Nandy, A.; Zhou, F.; Huang, W.; Xiao, J.; Seol, B.; Lee, J.; Fan, J.; Pommerenke, D. "Full-Wave Simulation of an Electrostatic Discharge Generator Discharging in Air-Discharge Mode Into a Product " IEEE Trans. EMC, Vol.99, 2010, pp. 28-37

Chapter 6: Summary and Conclusions

Robert Ashton, ON Semiconductor
Charvaka Duvvury, Texas Instruments
Alan Righter, Analog Devices

6.0 Introduction

This white paper has sought to capture the state of the art in system level ESD test and design and plot a course which will lead to improved system level ESD robustness while reducing the costs and effort to obtain this robustness. While today there is considerable knowledge of system level ESD, it is far from a mature science, and system level ESD design is often done with rules of thumb, trial and error and a combination of good and bad luck. Some of the design methods established in this paper seeks to minimize the often *ad hoc* approach to achieve system ESD robustness. This final chapter of the white paper will summarize what has been learned in the previous chapters and outline the advances which need to be made in the field.

6.1 Overview of ESD Stressing and System Response - Chapter 2

There are a number of system level ESD tests for different classes of products and applications. Most tests are based on the IEC 61000-4-2 ESD standard. The common elements of the test methods are to stress the completed systems with an ESD pulse source (ESD gun) using a combination of contact and air discharge directly to the system and indirectly to the coupling planes adjacent to the system under test. The tests look for both hard, physical, failures and soft failures in which system operation is interrupted. These tests are obviously very effective, since most electrical systems on the market have sufficient ESD robustness that the average system users are unaware of the threat from ESD.

The challenge today is when systems fail the ESD tests, usually during system qualification. Determining the path of the ESD stress of a hard failure is relatively straightforward since there is the physical damage of the failure. Diagnosing soft failures is much more difficult. In recent years there have been significant advances. There are now scanning technologies which can be used for diagnostics. These technologies can be classified into two general methods. In the first method, the ESD stress which leads to a failure can be applied repeatedly to a circuit board; probes sensitive to voltage or current scan the board surface to measure the path of the stress though the board. In the second method, probes which can inject electric or magnetic fields are scanned over the surface of a functioning circuit board to find where on the circuit board there is sensitivity to the applied fields.

These methods can be very effective in finding susceptible locations on a circuit, but they can be very labor and capital intensive. Scanning techniques are also most effective on designs with a known ESD or EMC weakness. It would be much more effective to be able to design a system to be robust the first time, rather than have to debug a failing system. Improvements in system design techniques are needed to avoid the need for debugging failures.

6.2 State-of-the-Art ESD/EMI Co-Design - Chapter 3

ESD/EMI design is similar to most design problems, requiring a balance between often conflicting goals. In ESD/EMI design, the conflicting goals are performance, robustness and cost. ESD/EMI design consists of identifying exposed and susceptible internal nets, evaluating the pulse entry point and selecting the components and layouts that will create a robust design. The design processes used to meet these goals will vary based on the complexity of the design, the experience of the designers and the available design resources. ESD/EMI design styles can be divided into practical and theoretical approaches. Each approach can range from very basic to comprehensive as illustrated in Table 4, (reproduced from Chapter 3).

Table 4: Practical and theoretical co-design methodologies for ESD/EMI robustness

		Methodology Type	
		Practical	Theoretical
Complexity & Cost	Basic	Designer's experience, lessons learned, design reuse	Datasheet comparisons
	Advanced	Component qualification testing	SPICE modeling of ESD injection
	Comprehensive	Rigorous head-to-head system level iterative testing	Full 3D Maxwell Field-Solver Simulations

As computer power has increased and electrical components and systems have become more complex, there has been a movement in design toward the use of more theoretical computer based simulations during the design process. The progress toward a theoretical approach is hampered in the ESD/EMI field by a lack of fundamental information available to the designer. This exists not just at the Full 3D Maxwell Field-Solver level but also at the SPICE modeling and even at the datasheet comparison level.

At the datasheet level, different manufacturers specify the protection properties of TVS components in very different ways. ESD survival levels are often quoted as an IEC 61000-4-2 voltage while others quote a voltage but do not reference the standard used for the test. Dynamic on-resistance of the components in the on state are often measured with different methods such as TLP or an IEC 61000-4-5 8/20 µs pulse; however the resistance measured from one method to the other is likely to differ dramatically. Most datasheets, however, do not specify a dynamic resistance at all. The datasheets for the integrated circuits requiring protection are even less helpful. Some integrated circuit datasheets do quote IEC 61000-4-2 survival levels for some interface IO pins. Integrated circuit datasheets often specify ESD robustness levels for HBM and CDM as well. The HBM and CDM tests are relevant for component handling during system manufacture; however, they are very misleading for predicting system level ESD performance. The relevant information of turn-on voltage or breakdown voltages and dynamic on-resistances are never quoted on datasheets and are often not known by the manufacturer of the circuit.

Attempting to do SPICE modeling is even more problematic. SPICE models are seldom available from manufacturers for TVS components. SPICE models of the properties of an integrated circuit appropriate for use in a system level ESD simulation are even rarer. A critical need in the ESD design environment is learning the properties of electrical components which are important during a system level ESD event. It is also important that the form of this information be similar from

supplier to supplier so that meaningful comparisons can be made. The component information must also be in a form that is appropriate for the tools being used. A SPICE model may not be much help to a designer looking for a simple datasheet comparison but is perfect for a designer wanting to do a circuit simulation.

A standardized specification for data, characterizing electronic components in the system ESD range of currents, voltages and stress duration, is a high priority. The format that such a specification should take depends critically on the tools that will use this information. There may need to be more than one format. The most basic format would be standardized datasheet parameters. Next would be a specification for high current SPICE models for TVS components and integrated circuits appropriate for circuit modeling of system level ESD events. The same would apply to passive components in the ESD mitigation path like ferrites. The appropriate form needed for 3D field simulations may need to be developed as this method of simulation matures.

6.3 Reference Methodologies for IC/System - Chapter 4

In White Paper 3 Part 1, the Industry Council on ESD Target Levels introduced the SEED concept and this document has been expanding on this concept. Developing more systematic approaches to system level ESD design has required the understanding and classification of how ESD can interact with the system and damage or interrupt system performance. The types of stress which can cause ESD issues are listed below.

- Category 1: High energy stress which can lead to physical failure
    - Category 1a: Stress delivered to IC from galvanic conduction
    - Category 1b: Stress delivered to IC without a direct galvanic path
- Category 2: Stress entering IC substrate which can cause latch-up or upset
- Category 3: Low energy pulses coupled to IOs which may cause upset

The system design techniques required to deal with each type of stress can differ. Understanding that the approaches need to be different is a first step toward defining an efficient co-design strategy. It is also important to know the limitations which various design approaches will have.

The classic SEED approach, as described in White Paper 3 Part 1, is directly applicable to the Category 1a stress. For Category 1a the stress entry point, current paths and susceptible circuits can usually be identified based on the standard circuit diagrams for a system. It is then conceptually straightforward to model the system's response to the ESD stress. This does not mean, however, that the Category 1a stress condition is totally understood and easily modeled. The major bottleneck today, as pointed out earlier in this chapter, is the lack of model files for sensitive ICs and TVS components.

Category 1b can also be addressed with the SEED approach, with the added requirement of understanding how the high energy stress enters the system. Identifying the entry path can be a challenge and is easiest to determine if the time and circumstances of failure are well known. Indirect high energy stress of a system can result from several events, such as:

- ESD stress to a metal case which then arcs to a sensitive circuit node
- ESD stress to an IO line which induces a large transient, either capacitively or inductively, to a nearby internal trace.
- ESD air discharge to a keypad or seams in the plastic case of a system
- Coupling of energy from a system housing ESD strike into internal IC bondwires

Once the entry point of the stress is identified it is possible to use the same SEED techniques as used for Category 1a stress. The additional information needed is a model for the input path. This could require a model for an arc between the ESD source and the entry point on the PCB or a capacitive or inductive model for the coupling between signal traces on the PCB.

Being able to design to protect against Category 2 stress requires an understanding of how current injected into the substrate of an IC can cause upset or latch-up. Today, there are no accepted methods for characterizing integrated circuits for their behavior when current is injected into their substrate. Development of such a test method and then how to model the ICs response is needed before Category 2 stress behavior can be predicted.

Category 3 stress levels are similar to the stress levels for EMC compatibility and advances in the robustness for EMC will also make systems more robust to lower energy strikes from low level ESD stress.

6.4 Standard Model and Analytical Tool Needs to Support SEED - Chapter 5

As has been discussed numerous times in this chapter and document, the ability to predict the behavior of systems to ESD stress requires detailed knowledge of the behavior of integrated circuits and TVS components in the voltage, current and time domain of ESD events. This component understanding must also be in a form which can be used by simulation tools used by system designers. SPICE models have been mentioned numerous times in this document. SPICE models are used for system and board design but are not the only tool. IBIS (Input/output Buffer Information Specification) models are used extensively for system and board design. IBIS models do not presently have the necessary features required for ESD system design. The necessary additions to the model need to be defined and procedures developed for extracting the relevant parameters from integrated circuits, TVS components and other components as well as the necessary PCB parameters such as coupling between traces.

The primary tools for determining component properties in the ESD range of voltage, current and time are standard and very fast TLP test methods. Standard TLP, with pulse lengths of 100 ns, is the ideal tool for obtaining I-V curves that describe component behavior during the long second peak of a system level ESD pulse, which carries the bulk of the energy of an ESD stress. VFTLP uses pulses in the range of 2 to 5 ns which have rise times similar to or faster than a system level ESD stress. VFTLP produces I-V curves which are characteristic of a component’s performance during the initial current spike of a system level ESD event. VFTLP can also be used to look at the time dependence of ESD protection circuits and components within the critical first nanosecond of an ESD event.

The TLP and VFTLP tools are of no use, however, if the needed component properties are not well defined. The behavior of TVS components, which can often be analyzed as two terminal

components, may be straightforward. One area that will need improvement is the analysis of the turn-on characteristics of TVS components. The requirements for integrated circuits are more complex. The important current paths within an integrated circuit may not be well defined. Power and ground pins are usually thought of as being very isolated nodes. The large power-to-ground capacitors, which are routinely placed to filter out power noise spikes in a system, will look more like a short to an ESD pulse than separate nodes. Chapter 5 showed how TLP curves for an IO vary depending on how power and ground pins are handled. The correct measurement conditions for predicting integrated circuit behavior during a system ESD event will require more experience than is available today.

6.5 Application Specific Information on System ESD Related Tests and Their Targets – Appendix A

Different product applications are used in a number of varying environments, and as such have different system ESD test standards tailored to those environments. Similar design strategies for ESD should be applicable across the application spaces, but the varying requirements and environments must be taken into consideration. Most test methods for system level ESD are based on IEC 61000-4-2. Some applications might benefit from re-evaluation of the particular ESD test method use to better match use and stress environments.

For example, mobile phones are covered by a wide variety of EMC standards, but most ESD testing is done using IEC 61000-4-2. Testing of small hand held devices based on IEC 61000-4-2 may give a different stress than actual stress in their normal environment, and might need some updating, since the IEC test standard was developed with an assumption of a table top system, rather than a portable system which is typically used when electrically floating.

The automotive industry is one which has developed a test standard, ISO 10605, which is substantially modified from IEC 61000-4-2. Automotive electronics also operate in an electrically noisy environment and are very susceptible to coupling of signals due to long wiring harnesses and a multitude of separate electronic control units (ECUs) distributed throughout the vehicle.

The avionics industry is even more susceptible to coupling between systems due to the very long lengths of wire harnesses which exist in modern aircraft. The electrical environment is also rapidly changing in the aircraft environments as airplanes are increasingly using new materials and moving more and more to electrical control of the aircraft.

The challenge is to enable by SEED a common, unified design approach, which can be used across the industry, allowing optimum use of devices and minimizing cost and time to market.

6.6 Technology Roadmap and Direction – Appendix B

Even as better methods for system level protection are understood and implemented in a more optimized manner, technologies will continue to advance at a faster rate. As an overview, these advances in IO speeds, broader system applications, and innovative developments from 3D IC packages to complex integration of multiple functions on a single board make the continued demand of IEC protection even more challenging. But at the same time there are other innovations such as optical interconnects and polymer transient suppressors that can alleviate

some of these difficulties. However, the real sense of the IEC requirements needs to be understood and perhaps revised in the context of where the trade-off begins to play a role in performance versus robustness.

Looking more into details, the ever-increasing circuit complexity and scaling of silicon integrated circuit technologies is placing increasingly severe restrictions on the effectiveness of system level ESD protection components, and design methodologies employing these new circuits. Analysis of the present state-of-the-art in technology as well as a forecast in technology trends in the components which make up a system, along with the use of methods described in this document, is critical to system level ESD success in future systems.

Advances in IC technology from the present state-of-the-art at the 40 nm process node to the 22 nm process node and beyond are forecast in the next five years. The gate oxide breakdown voltages in these technologies are comparable to junction breakdown voltages, and circuit ESD protection paths must be carefully designed to maintain the ESD levels above those levels which the assembly factories can guarantee by ESD factory control. It is critical as well that IO and power supply protection continue to advance at the lower operating voltages to allow efficient system level ESD protection. Faster circuit speeds resulting from these technology advances will lead to faster IO bus protocols. USB frequencies of 15-20 Gbit/s will place increasingly severe limits on the range of system level protection that can be used. HDMI, which has the additional requirement of minimal signal swing at 3-6 GHz operation, will also see an increasingly severe environment for system ESD.

Regarding advances in automotive technology, the trend of increasing use of electronics to make automobiles safer and user-friendly will continue. The electronics in automotive systems tend to lag in technology behind their computer technology counterparts by 1-3 process generations. However, technologies of 65 nm and up will be increasingly used in automotive electronics in the next five years in applications such as digital signal processing (DSP) in audio systems, micro-electrical-mechanicals (MEMs) devices, voltage regulators and LIN / CAN automotive communication networks.

Advances in packaging technology resulting from 3D interconnects (such as through silicon vias (TSVs)) connecting multiple IC overlapping die, as well as enabling more portable system on a chip circuitry, will make system level ESD protection and failure diagnosis more difficult. More efficient scanning and diagnosis techniques such as those described in this document will go a long way towards improvement of system level ESD protection for both hard and soft failures. One of the complex issues for future technology will be the EMI effects of stacking die. In the case of two die or three die stacking, the dominant effects on EMI coming from the interposer design and the die to die coupling needs to be considered. These become more complex as multiple die are stacked and could greatly impact the design of system level ESD protection in future applications.

Although traditional FR4-based boards and surface mount technologies will continue to dominate the system board / interconnect market, advances in board and interconnect technology such as molded interconnection device (MID) for 3D board design and roll-to-roll (R2R) flexible system board technology will become more common. These new methods for integration of system level ESD protection technology in new system environments will become a development priority.

Polymer-based ESD suppression components are also finding new applications in system level ESD protection. Although their turn-on characteristics and component operating characteristics can vary with multiple ESD strikes, they are finding applications as secondary protection for existing system ESD protection strategies.

Finally, it can be said that system level ESD design will continue to ride the wave of technology developments into the future. While developments that may relieve system exposure to ESD threats will occur, the advances and complexities of system design may outweigh these design developments; with the net effect that the system level ESD design will continue to become more challenging as the system performance level increases. Thus, one might still need to consider the following: "What is the required "correct" level of system level ESD robustness for an application?"

6.7 Outlook

System level ESD will continue to be a challenge in the future, but as this white paper has shown, there are a number of techniques which can be used to improve the success rate of system level ESD design. Tools such as TLP and VFTLP should be used to understand the properties of both sensitive circuits and the components used to protect them. Scanning tools, as explained in Chapter 2, provide useful insight into the stress propagation on boards and within systems and enable detection of sensitive circuit nodes. These tools will not reach their full potential unless the data they collect can be used within the standard design flow for an electronic system. This requires that design tools can use the additional ESD data obtained from TLP measurements and scanning tools. EDA vendors must therefore enhance their tools to use the new information. Model files such as IBIS and SPICE, which describe the electrical properties of components, need to include the description of component behavior in the ESD range, which is well beyond normal operating range. Suppliers of components, from integrated circuits to ESD protection components, also need to characterize their products in the ESD range. This characterization must be compatible with the EDA tools and enhanced model files. None of this will happen without a great deal of communication between EDA tool vendors, component suppliers and system designers. This white paper, however, provides a major step towards understanding the technical challenges. Based on this, the industry can move forward to an aligned system level ESD design concept assuring a high first pass success rate at minimum system cost.

Appendix A: Application Specific Information on System ESD related Tests and their Targets

Harald Gossner, Intel Corporation
Leo G Henry, ESD-TLP Consultants
Ghery Pettit, Intel Corporation
Wolfgang Reinprecht, Austria MicroSystems
Pasi Tamminen, Nokia
Vesselin Vassilev, Novorell
Joost Willemen, Infineon

A.0 Introduction

This Appendix addresses the typical stress conditions and design solutions used in various electronic systems including mobile phones, medical devices, computers, consumer electronics, automotive components and avionics. It provides an overview of interference test standards to be applicable beyond even IEC 61000-4-2, and discusses the impact of the multiple stress requirements on the design solutions. In addition, the applicability of the previously introduced SEED concept is analyzed for the various types of systems.

A.1 System Tests and Targets of Mobile Phones

A.1.1 Overview of System ESD Related Mobile Phone Tests

ESD qualification is part of the suite of EMC tests for mobile phones. EMC/ESD immunity and emission acceptance tests are based on international and national standards. These standards specify measurement setups, frequency ranges and corresponding acceptance limits. Over 40 standards for immunity and emission qualification exist for mobile phones. A number of these commonly used standard families are listed below:

- IEC 61000-4-2 [1]
- CFR 47 §xx.xx [2]
- EN 300 xxx [3]
- EN 301 xxx [4]
- EN 55020 [5]
- EN 55024 [6]
- TS 25.xxx [7]
- TS 36.xxx [8]
- TS 51 xxx [9]
- TS 151 xxx [10]
- GBT 22450.1-2008 [11]
- YDT 1592.1 [12]
- PTCRB NAPRD.03 [13]

Mobile phones can be exposed to all possible hostile environments where people move. However, strong direct ESD discharges from the environment through the mobile phone to the earth ground are not common as mobile phones typically are not grounded during operation. There is a greater possibility to experience discharges between a phone and a person and between the phone and a cable (CDE). To guarantee operation over these environments, phone ESD acceptance tests are performed in the worst scenario environment where the phone is close to the earth and may have also high inductive ground cables in place.

Mobile phone system and device level ESD measurements are adopted from the ETSI standard, ETS 300 342-1 [14]. The standard stress for electrostatic discharge is IEC 61000-4-2, and typically level 4 requirements must be fulfilled with the end products. In the IEC 61000-4-2 test setup, the mobile phone is placed on a table in different positions and has a charger and accessory cables attached. The phone is typically in connection with a base station and operation is monitored in real time during the stress tests. Contact discharge testing to conductive surfaces of the system and to coupling planes is performed at 8 kV. Lower stress levels are also commonly tested, from 1 kV upwards. Air discharge testing to insulated or non-conducting surfaces is performed up to 15 kV. Each stress point is stressed multiple times with both polarities. Figure A1 depicts the two principle testing methods of contact and air discharge. The total ESD strike count is typically hundreds of pulses.

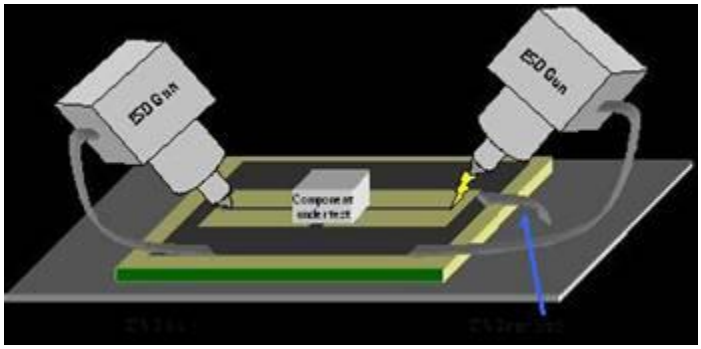


Figure A1: Principle picture of contact and air discharges with an ESD gun often used to characterize PCB designs during development

System level ESD testing is often required for those IC components themselves, within the mobile phone, which have interface pins. Interface connections with single devices are qualified with the system level ESD waveform by using case specific test boards. The test board must have all the important transmission lines; antenna, transmitter (TX), receiver (RX), control, power supply and ground connections in place. The test board can also have all those external components in place which are needed for the IC components' operational testing between the stress pulses.

A.1.2 State of the Art System Design Concept

The main challenge with mobile phones is to meet the system level EMC requirements. The product itself contains several radio systems which have to operate simultaneously without disturbing each other. There may be 4 to 6 additional radio-antenna sub-systems within the phone operating at the same time in a very small space. The main purpose of system level EMC design is to get product internal and external EMC challenges under control. Also, certain interface pins and covers may get direct ESD discharges which may disturb system operations.

ESD protection can be divided into two main areas, interface pin protection and indirect / direct ESD/EMC stresses on the cover area.

A.1.2.1 Interface Pin Protection

Interface pins, which are directly stressed in a mobile phone, have both on-board and on-chip protection for system ESD protection. On-board protection components also contribute to EMI attenuation. Interface connections include USB, HDMI, subscriber identity module (SIM) card, accessory connector, audio plug, memory card and charger plugs. These connections require case specific matching, and here simulation tools and SEED is the most beneficial way to optimize the design.

A.1.2.2 Indirect and Direct ESD/EMC Stress on the Cover Area

ESD/EMI can leak inside the phone when product covers are stressed with IEC 61000-4-2 contact and air discharges. Covers have gaps and the air discharges can leak inside through the openings. Metallic parts (covers, decoration marks, frames, etc.) may also transmit RF noise onto electronics and cause EMI problems. These challenges are typically controlled with detailed design rules for mechanics and grounding principles. Some internal and interface connections can also get extra stress when discharge energy conducts or radiates onto board traces. Another way to estimate EMC/ESD noise levels is to use 3D simulations where the mechanics and the stress waveforms are modeled in detail.

A.2 System Tests and Targets of Automotive Electronic Components

A.2.1 Overview of System ESD Related Automotive Electronics Tests

Automotive ECUs are subjected to numerous tests to ensure proper functionality in the particularly hostile vehicle environment.

The first group of tests is based on the test specs that are issued by standardization bodies. These publicly available standards define test methods and test stress criteria; however, pass/fail limits are not fixed by these documents but depend on the particular application. In addition many OEMs and Tier 1 suppliers have developed their own “in-house” spec or “consortium” specification documents. These documents often refer to the above mentioned public test specs, but also contain the required pass/fail limits for the particular application.

First, the public specs will be discussed. For system level ESD, two test standards are applicable:

1. IEC 61000-4-2 *Electromagnetic compatibility (EMC)—Part 4: Testing and measurement techniques—Section 2: Electrostatic discharge immunity test*. This document defines which ESD tests are to be applied to electronic equipment in general.
2. ISO 10605 [15] – *Road vehicles – Electrical disturbances from electrostatic discharge*. This document defines which ESD tests are applied to components for vehicles as well as vehicles.

The ESD generators used in both test specs are similar. ISO 10605 defines two different discharge networks for testing against ESD stress from persons outside or inside a vehicle. Although both test specifications define that ESD zaps should be applied to all kind of surfaces that can be touched by a user, often the same test methods are being used to stress individual pins of electronic components (i.e. ECUs, sensors).

In addition to ESD tests, various other EMC tests are required. There are differences between tests that are applied on the IC level and tests that are applied to the system level component (ECU, sensor) and the ECU-system level (ECU with peripheral). The expectation of the component level tests is that if a component is EMC robust, the system built with this component will be EMC robust as well, which is not the case.

Examples of IC level EMC tests are:

- IEC 61967 [16] – *Integrated circuits - Measurement of electromagnetic emissions, 150 kHz to 1 GHz*
- IEC 62132 [17] – *Integrated circuits - Measurement of electromagnetic immunity, 150 kHz to 1 GHz*

Examples of system level EMC tests are:

- ISO 7637 [18] – *Road vehicles – Electrical disturbances from conduction and coupling*.
- ISO 16750-2 [19] – *Road vehicles – Environmental conditions and testing for electrical and electronic equipment – Part 2: Electrical loads. Start profile/load dump, formerly part of the ISO 7637 standard (test pulse 4a, 4b, and 5).*
- CISPR 12 [20] – *Vehicles, motorboats and spark-ignited engine-driven devices – Radio disturbance characteristics — Limits and methods of measurement*
- CISPR 25 / EN 55025 [21] – *Radio disturbance characteristics for the protection of receivers used on board vehicles, boats, and on devices - Limits and methods of measurement.*
- ISO 11451 [22] – *Road vehicles – Vehicle test methods for electrical disturbances from narrowband radiated electromagnetic energy*
- ISO 11452 [23] – *Road vehicles – Component test methods for electrical disturbances from narrowband radiated electromagnetic energy*

The different parts of the Society of Automotive Engineers (SAE) J1113 standard [24] describe equivalent test methods, as in the above mentioned standards, and are commonly used by the US automotive industry. The ISO standards are referred to in the SAE J1113 documents.

The Automotive Electronics Council (AEC) has compiled (in the AEC Q100 group of standards [25]) many stress tests applicable to automotive systems and components. Included are ESD and EMC tests, however, system level ESD testing is presently not a standard within AEC Q100. The test methods refer mostly to public test specs as mentioned above. But in the case of device level ESD tests, AEC Q100 provides its own test method, which is different in detail compared to the commonly used JEDEC and ESDA standardized tests.

Numerous car system suppliers and car makers have issued their company specific ESD and EMC requirements. For example, Ford's specification is publicly available under www.fordemc.com [26, 27]. In other cases, Tier 1 or OEM consortia issue joint specification documents. For example:

- Generic IC EMC Test Specification. Bosch, Infineon, Continental (BISS)
- OEM Hardware requirements for CAN, local interconnect network (LIN) and FlexRay interface (consortium of German automotive OEMs) [28].

These documents refer mostly to public test specifications and also contain specific pass/fail requirements. For the most part, these documents are not publicly available.

A.2.2 State of the Art System Design Concept

Considerable effort in IC and ECU development is done to meet stringent system level ESD requirements included in the EMC qualification of ICs and ECUs. To discuss the commonly used strategies in the system design for EMC, it is necessary to differentiate between different interface pin categories. The following categories illustrate the main strategies for protecting different pin types in typical automotive ECUs. The applicable strategy followed depends on the functionality of the pin in question.

1. Supply lines (connected to the car battery):
   a. Local (PCB level) load dump clamps
   b. Reverse polarity (due to reversal of battery connection) protection diodes
   c. Supply line decoupling capacitors
   d. System level ESD protection clamps (TVS, varistors)

2. Power switches (connected to electromechanical actuators and indicator devices, such as lighting bulbs, motors, relays, displays, etc.):
   a. Self protecting switches: Power output switches which are large enough to divert system level ESD zaps
   b. Board level EMC capacitors: If switching speed allows usage of EMC capacitors at the switch output, they contribute to diverting system level ESD zaps
   c. System level ESD protection clamps: TVS diodes and varistors, for example, must be used if the switching device is not robust against system level ESD zaps

3. Transceiver buses (LIN, CAN, Flexray automotive communication bus systems):
   a. IC level ESD protection: Many transceiver devices or integrated transceiver modules are equipped with IC-internal system level ESD clamps
   b. System level ESD protection clamps: Are to be added if the IC-internal ESD protection is not sufficient for system level ESD zaps
   c. Common mode chokes: Applied to reduce EMC, may have influence on robustness against system level ESD zaps

4. Other IOs (for instance, sense lines):
   a. EMC capacitors
   b. TVS diodes
   c. RC networks

In addition to protection strategies for the individual pins of an ECU, the board level design (especially the layout of ground planes) has significant influence on the system level ESD and EMC properties. Ford has published a good introductory guideline document entitled "EMC Design Guide for Printed Circuit Boards" which is available from www.fordemc.com.

A.3 System Tests and Targets of Computing Devices

A.3.1 Overview of System ESD Related Computing Device Tests

Computing devices, also known as information technology equipment (ITE), are subject to the immunity requirements in CISPR 24:2010 [29]. CISPR 24 has specific requirements for, among other items, ESD testing. The test methods in IEC 61000-4-2:2008 are called out with the following specific requirements:

- Contact discharge testing to conductive surfaces of the device and to coupling planes is performed at 4 kV IEC. No lower levels are required.
- Air discharge testing to insulated or non-conducting surfaces is performed up to 8 kV IEC. Lower levels are also evaluated.
- The performance criteria for ESD testing in CISPR 24 is "Performance criterion B". The basic requirement is that "After the test, the equipment under test (EUT) shall continue to operate as intended without operator intervention." The EUT may react to the ESD event (for example, a pop heard in a speaker), but it must self-recover without help from the operator.
- Electrostatic discharges are only applied to points and surfaces of the EUT which are expected to be touched during normal operation, including user access as specified in the user manual.
- Discharge to contacts of open connectors is not required.

A.3.2 State of the Art Design Concepts

Typically the only special design features used on ITE products for ESD protection are diodes on IO ports to shunt ESD currents to ground to protect circuitry from damage.

A.4 System Tests and Targets of Medical Electronic Components

A.4.1 Overview of System ESD Related Medical Electronics Tests

A medical device is an electronic component which is used for medical purposes for patients in diagnosis, in therapy and/or in surgery. Medical devices include a wide range of products varying in complexity and application. Examples include, but are not limited to, medical thermometers, blood sugar meters, X-ray machines, pacemakers, hearing aids, and heart rate machines.

The strict requirements for medical devices are set forth by the Food and Drug Administration (FDA). Risks are related to reliability and duration of use. The standard quoted for medical devices is ISO 14971:2007 [30], which specifies processes to identify hazards and evaluate risks associated with the lifecycle of medical devices. FDA requirements for these products, record keeping and reporting, are included/contained in Title 21 Code of Federal Regulations Parts 1000-1299 (21 CFR 1000- 1299) [31]. Medical devices emitting radiation are subject to the provisions

of the FD&C Act and listed in 21 CFR 1000.15 [32]. Radiation emission includes ionizing electronic radiation, particulate radiation, ultra violet (UV), visible, infra-red (IR), microwave, radio and low frequency, laser, infrasonic, sonic and ultrasonic.

Medical Device and equipment testing include product safety compliance, EMC compliance, and FDA Guidance Documents and consensus standards necessary for FDA clearance, including IEC 60601 [33], American Society for Testing and Materials (ASTM), ISO and Association for Advancement of Medical Instrumentation (AAMI) standards. Associated standards are: UL 60601-1, CSA C22.2 No. 60601-1, EN 60601-1, EN 60601-2-XX, IEC 60601-1, and IEC 60601-2.

IEC 60601 is a series of technical standards for the safety and effectiveness of medical electrical equipment, published by the IEC. First published in 1977, IEC 60601 is now a widely accepted benchmark for medical electrical equipment and compliance. As of 2011, the IEC 60601 consists of a general standard, about 10 collateral standards (IEC 60601-1-X), and about 60 particular standards (IEC 60601-2-X), and the standard includes a process for Certification.

The general standard ***IEC 60601-1 - Medical equipment/medical electrical equipment - Part 1: General requirements for basic safety and essential performance*** - gives general requirements of the series of standards. This IEC 60601-1 standard applies to all medical products which are not implanted inside the human body.

Collateral standards (numbered IEC 60601-1-X) define the requirements for certain aspects of safety and performance, such as Electromagnetic Compatibility (IEC 60601-1-2); or Protection for diagnostic use of X-rays (IEC 60601-1-3) or *IEC 60601-1-9* for Environmentally Conscious Design of Medical electrical Equipment. This Part 9 standard asks manufacturers of medical to consider the environmental impacts of their devices throughout the product's entire life cycle and to minimize these where possible. Medical EMC testing is typically performed in accordance with EN/IEC 60601-1-2 for most devices. IEC 60601-1-2, a collateral standard, states that the ESD requirements are +/- 2, +/- 4 and +/- 8 kV air discharge 12 (to non-conductive accessible surfaces) and +/- 2, +/- 4 and +/- 6 kV contact discharge (to 13 conductive accessible surfaces).

Particular standards (numbered 60601-2-XX) define the requirements for specific products, such as MR scanners (IEC 60601-2-33). IEC 60601-2 is Part 2 and addresses specific requirements for a particular type of medical devices. There are over 40 Part 2 devices. The XX is a number from 1 to 40+, representing the applicable Part 2 device. Additions and/or deviations to the requirements of EN/IEC 60601-1-X are published in the appropriate EN/IEC 60601-2-XX for particular devices.

In order to market medical devices within the member countries of the European Union, a product must comply with the essential requirements of the medical device directive (MDD) 93/42/EEC [34]. Compliance with harmonized standards (such as EN 60601-1-2:2001 for EMC, and EN 60601-1 for electrical safety) provides conformity to specific requirements.

Medical device testing also includes static, dynamic, fatigue, wear testing and failure analysis on medical devices and orthopedic implants according to ASTM and ISO standards.

A.4.2 State of the Art System Design Concept

EMC is a major concern and design challenge in medical electronics, as the consequences of any malfunction may be life threatening [35]. Design constraints, notably leakage current limitations for some devices, make the EMC design of medical electronic devices more difficult than their non-medical counterparts. Typical EMC design practices include shielding and filtering.

A.5 System Tests and Targets of Avionic Components

A.5.1 Overview of System ESD related Avionic Component Tests

EMC/EMI robustness is primarily considered for the on-board service electronics (avionics) in the aerospace industry. Long wiring (total wire lengths of several km are typical for the aircraft architectures) is susceptible to picking up EM noise from the environment and transferring the generated impulses to the avionic components. This can lead to a disturbance of electronic component operation, or a functional failure. The typical failure during an ESD event in aerospace (from a system point of view) originates from field induced transients. The most commonly referenced IEEE surge standards used in practice are:

- IEEE C62.41.1 [36] – *2002(IEEE Guide on the Surge Environment in Low-Voltage (1000 V and Less) AC Power Circuits)*
- IEEE C62.41.2 [37] – 2002 *(IEEE Recommended Practice on Characterization of Surges in Low-Voltage (1000 V and Less) AC Power Circuits*)
- IEEE C62.45 [38] – 2002 (*IEEE Recommended Practice on Surge Testing for Equipment Connected to Low-Voltage (1000 V and Less) AC Power Circuits*)

IEC 61000-4-2 is used as the ESD standard model at the board level. However, actual in-flight or in orbit conditions (humidity, temperature, pressure, etc.), which affect the surge waveforms compared to those on ground level, are not covered by this.

Other standards in use for EMI robustness at the component level are: MIL-STD-461 [39] (military), RTCA DO-160 [40], and EUROCAE ED-14 [41] (commercial). The aircraft level standards include US Military MIL-STD-464 [42], RTCA DO-160 and EUROCAE ED-14.

A.5.2 State of the Art System Design Concept

In the aerospace industry, for various practical reasons, a typical system design strategy is to consider the protected ICs very sensitive to ESD events.

The most common technique used at present to protect avionics is the placement of so–called "surge protection devices" (SPDs) at the power and IO lines of each sub-system. These SPDs are designed to act as filters, and can either be discrete devices or circuits, turning on at specific overvoltage or frequencies according to the overvoltage/overcurrent transient characteristics.

A particular issue to be addressed in the present and forthcoming protection/design approaches is the introduction of composite materials for the aircraft body and/or the penetration of non-conforming and/or counterfeit materials and components (which have virtually "unknown" properties related to EMC/EMI/ESD). All of these factors introduce a variety of unknowns related

to the stress waveforms seen by the avionics system and impact their susceptibility and robustness to the generated overvoltage/overcurrent transients.

A.6 System Tests and Targets of Consumer Electronic Devices

A.6.1 Overview of System ESD Related Consumer Electronics Tests

Consumer electronics covers quite a wide range of devices, and the scope in this appendix will be limited to components of audio/video equipment, such as TVs, camcorders, MP3s, iPods, and mobile displays for example. In general, test methods according to IEC 61000-4-2 are used to perform contacted, air, and indirect discharge. The level of robustness depends on the environment in which the product is used and the incidence of human handling. The following test methods and specific requirements generally apply:

- IEC Contact discharge testing - to conductive surfaces of the device and to the interface pins which can be touched by humans during production and handling of the final product. 8 kV is a common level for portable products and ports often handled by humans, and 4 kV for products not in human contact.
- IEC Air discharge testing - to isolated or non-conducting surfaces and connectors is performed up to 15 kV. Discharges to displays, keyboards, etc must not cause the product to stop functioning.
- Indirect IEC discharge to metal planes (horizontal/vertical) on which the product is located to ensure functionality during operation. Levels of 8 kV contact and 15 kV air often apply. This test is done in an operating mode to check the immunity to the electromagnetic fields.
- Specific test for light emitting diode (LED) TV: CISPR 13 Class B [43]
- Handheld Audio applications also require:

    1. EN 55022
    2. EN 55024
    3. IEC 61000-4-2, -4-3, -4-8

Beside international standards, there are various examples for company specific testing:

- CDE robustness - tested by system level ESD pulses to system ports which are not specified by IEC 61000-4-2.
- Charged board event (CBE) testing - to simulate the discharge from a CBE or charged modules, caps of 100 nF – 800 nF are precharged with 25 V - 40 V and then discharged to the pin under test. This could be an exposed IC pin (Feedback) or the OUT-pin of the controlled external power.
- Stress testing of a powered IC - tested by applying MM-type pulses up to 300 V to check the sensitivity of a device through onboard coupling of an external pin to an internal pin because of the board wiring. Typically, stressed pins are control and feedback pins for external power devices or pins connected to lines wired in parallel to signals going offboard.

- Discharge to contacts of open connectors for main interface ports (Audio/Video) - tested by applying MM-type pulses up to 300 V under operation. System interruption with recovery is acceptable.

A.6.2 State of the Art Design Concepts

To protect the exposed pins of the devices, large on-chip diodes to the supply rails are commonly used. If the integration of these very large on-chip protection devices is not possible due to performance reasons, external TVS diodes are placed on the board. For TV and other display driver components, the output pins are usually protected against GND, which must also be robust against various EOS/ESD stress conditions. System level ESD protection and test concepts are widely discussed for LCD applications [44-50].

In some cases, high CBE and CDE robustness of certain exposed pins are requested to prevent damage when connecting the display with the driver boards. Typically, large primary on-chip ESD protection devices are used and an extra-large external capacitance is connected to the supplies.

Consumer electronic devices often have a very tight material cost target, which forces the use of lower cost EMC/ESD protection methods. Protection by the mechanics is the desired approach. Additional basic passive chip components may be needed for residual ESD and EMC filtering. When enhanced protection is needed, onboard varistors, ferrites and diodes can be placed at the most critical signal lines. Even then, the target is to limit this to a minimum and later cost driven redesigns will lead to a removal of expensive ESD/EMC devices.

A.7 Applicability of System-Efficient ESD Design (SEED)

Basic SEED concepts, which provide a methodology to match board protection and IO behavior for prevention of damage, are applicable to a number of interfaces which can be exposed to direct or indirect ESD stress with large stress energy. They are usually protected by a combination of PCB clamping elements like TVS devices or varistors, and current limiting serial elements such as ferrite beads. Examples for these pins are listed in Table A-1.

Table A-1: Typical interfaces exposed to IEC stress

IC pin type	Exposure	Field of Application
USB	direct	mobile phones/computing
Headset	direct	mobile phones/computing
Antenna	direct	mobile phones
Battery	direct	mobile phones
Key pads	indirect	mobile phones
LIN	direct	automotive
CAN	direct	automotive
Flexray	direct	automotive
LAN	direct	computing
DVI	direct	computing
TV driver output	direct	consumer

A.7.1 A SEED Case Study for USB

Soft fails, which represent most of the observed fails during system development are related to an indirect stress path triggered by crosstalk or noise injection. In this case, the methods described as advanced SEED will be useful to optimize ground planes, pulse mitigating discrete elements, and PCB trace layout. It should be emphasized that the optimization of the mechanical layout of the case is not in the scope of SEED, while it plays an important role in the system ESD robustness. However, mechanical layout is often predefined by product design and functional limitations.

A possible design flow applying SEED for a USB 3.0 interface with challenging high speed requirements is discussed, focusing on the USB port as an entry point of the ESD pulse. The design of a high performance interface like USB 3.0 ranging up to 5 Gbit/s requires the knowledge of the complete transfer line from transceiver to receiver. The eye diagram at the receiving port is commonly taken as figure of merit. The design of the IO circuit needs an early definition of the maximum capacitive load by on-chip / on-board ESD protection elements and of the worst case serial resistance. The application of a basic SEED approach allows selection of an optimum TVS diode with minimum capacitance while still matching the high current IO characteristic. An optimization of PCB protection elements and serial filters for a USB (3.0) following the SEED approach is demonstrated in [51]. Based on this initial choice of protection and the draft of the PCB layout, the capacitive and inductive coupling to adjacent lines can be extracted and the level of cross-coupling can be simulated for an ESD waveform. The transient latch-up robustness of IOs exposed to induced current pulses determines whether the coupling must be reduced or mitigating elements need to be added to the victim lines. Also, changing the placement of the TVS diode will influence both cross coupling to adjacent lines and stress received by the USB pin.

In the next step, the supply noise level can be assessed by these simulations, as long as the supply RLC net on the board is appropriately modeled. If the amplitude in the noise power spectrum exceeds the sensitivity level of the IC, mitigating measures might be implemented such as reduction of resistance in the supply net or use of buffer caps. Finally, the impact on signal integrity has to be estimated.

Together with functional simulation of the transmission line, this allows a simulation based co-design of the function and ESD protection of a USB subsystem, taking into account IC behavior, board components and PCB layout.

References

[1] IEC 61000-4-2, 'Electromagnetic compatibility (EMC) – Part 4-2: Testing and measurement techniques – Electrostatic discharge immunity test', Ed. 2.0, 2008. -- http://webstore.iec.ch/
[2] CFR 47 §xx.xx -- http://www.access.gpo.gov/nara/cfr/waisidx_02/47cfrv2_02.html
[3] EN 300 xxx -- http://www.etsi.org/WebSite/Standards/Standard.aspx
[4] EN 301 xxx -- http://www.etsi.org/WebSite/Standards/Standard.aspx
[5] EN 55020 -- http://www.etsi.org/WebSite/Standards/Standard.aspx
[6] EN 55024 -- http://www.etsi.org/WebSite/Standards/Standard.aspx
[7] TS 25.xxx -- http://www.etsi.org/WebSite/Standards/Standard.aspx
[8] TS 36.xxx -- http://www.etsi.org/WebSite/Standards/Standard.aspx
[9] TS 51 xxx -- http://www.etsi.org/WebSite/Standards/Standard.aspx
[10] TS 151 xxx -- http://www.etsi.org/WebSite/Standards/Standard.aspx
[11] GBT 22450.1-2008 - - http://www.ptsn.net.cn/ (Chinese only)
[12] YDT 1592.1 - http://www.ptsn.net.cn/ (Chinese only)
[13] PTCRB NAPRD.03 -- http://www.ptcrb.com/
[14] ETS 300 342-1 -- http://www.etsi.org/WebSite/Standards/Standard.aspx
[15] ISO 10605 -- http://www.iso.org/iso/iso_catalogue.htm
[16] IEC 61967 -- http://webstore.iec.ch/
[17] IEC 62132 -- http://webstore.iec.ch/
[18] ISO 7637 -- http://www.iso.org/iso/iso_catalogue.htm
[19] ISO 16750-2 -- http://www.iso.org/iso/iso_catalogue.htm
[20] CISPR 12 -- http://webstore.iec.ch/
[21] CISPR 25 / EN55025 -- http://webstore.iec.ch/
[22] ISO 11451 -- http://www.iso.org/iso/iso_catalogue.htm
[23] ISO 11452 -- http://www.iso.org/iso/iso_catalogue.htm
[24] SAE J1113 -- http://standards.sae.org/
[25] AEC Q100 -- http://www.aecouncil.com/AECDocuments.html
[26] Ford Motor Company, EMC Design Guide for Printed Circuit Boards, Engineering Specification ES-3U5T-1B257-AA, http://www.fordemc.com/docs/download/EMC%20Design%20Guide%20for%20PCB.pdf
[27] Ford Motor Company, Electromagnetic Compatibility Specification for Electrical/Electronic Components and Subsystems, General Specification Electrical/Electronic, EMC-CS-2009.1, http://www.fordemc.com/docs/download/EMC_CS_2009rev1.pdf
[28] Audi, BMW, Daimler, Porsche, and Volkswagen, Hardware Requirements for LIN, CAN and FlexRay Interfaces in Automotive Applications, version 1.1, 2009.
[29] CISPR 24:2010 -- http://webstore.iec.ch/
[30] ISO 14971:2007 -- http://www.iso.org/iso/iso_catalogue.htm
[31] 21 CFR 1000- 1299 -- http://www.accessdata.fda.gov/scripts/cdrh/cfdocs/cfCFR/CFRSearch.cfm
[32] 21 CFR 1000.15 -- http://www.accessdata.fda.gov/scripts/cdrh/cfdocs/cfcfr/CFRSearch.cfm?FR=1000.15
[33] EN/IEC 60601-1-2 -- http://webstore.iec.ch/
[34] MDD 93/42/EEC -- http://eur-lex.europa.eu/
[35] W. Kimmel and D.D. Gerke: "Exploring systems EMC in Medical Devices", http://www.eetimes.com/design/medical-design/4212205/Exploring-systems-EMC-in-medical-devices
[36] IEEE C62.41.1 – 2002 – http://ieeexplore.ieee.org/
[37] IEEE C62.41.2 – 2002 – http://ieeexplore.ieee.org/
[38] IEEE C62.45 – 2002 – http://ieeexplore.ieee.org/
[39] MIL-STD-461 -- http://assist.daps.dla.mil/quicksearch/
[40] RTCA DO-160 -- http://www.rtca.org/downloads/
[41] EUROCAE ED-14 -- http://www.eurocae.net/
[42] MIL-STD-464 -- http://assist.daps.dla.mil/quicksearch/
[43] CISPR 13 -- http://webstore.iec.ch/
[44] Tai-Ho Wang; Wen-Hao Ho; Lin-Chien Chen; "On-Chip system ESD protection design for STN LCD drivers", EOS/ESD Symposium 2005, 8-16 Sept. 2005, pp. 1 - 7.
[45] Pavey, LD.; Kerr, J.; "ESD simulation and cure: a case study", ESD and ESD Counter Measures IEE Colloquium on 28 Mar 1995, pp. 1 -4.
[46] Ming-Dou Ker;Cheng-Cheng Yen; "Investigation and Design of On-Chip Power-Rail ESD Clamp Circuits Without Suffering Latch-up-Like Failure During System-Level ESD Test" IEEE Journal Solid State Circuits, Nov. 2008, Vol.42, pp. 2533-2545

[47] Ming-Dou Ker,Wan-Yen Lin1,Cheng-Cheng Yen1,Che-Ming Yang,Tung-Yang Chen,Shih-Fan Chen, "Protection Design Against System-Level ESD Transient Disturbance on Display Panels", 2010 Asia-Pacific International Symposium on Electromagnetic Compatibility, April 12 - 16, 2010, Beijing, China, pp. 438-441
[48] Cheng-Cheng Yen;Wan-Yen Lin;Ming-Dou Ker;Che-Ming Yang;Shih-Fan Chen;Tung-Yang Chen; "New transient detection circuit to detect ESD-induced disturbance for automatic recovery design in display panels", Design & Technology of Integrated Systems in Nanoscale Era (DTIS), 2011, pp. 1-4
[49] Xiao, J.; Pommerenke, D.; Drewniak, J. L.; Shumiya, H.; Maeshima, J.; Yamada, T.; Araki, K.; "Model of Secondary ESD for a Portable Electronic Product", IEEE Trans. EMC, Oct. 2011, pp. 1-10
[50] J.Xiang, D. Pommerenke et.al. "Model for ESD LCD Upset of a Portable Product", IEEE International Symposium on EMC, 2010, pp. 354-358
[51] S. Bertonnaud, C. Duvvury; "IEC System Level ESD Design for OMAPTM System", private communication (International ESD Workshop 2011, Lake Tahoe)

Appendix B: Technology Roadmap and Direction

Charvaka Duvvury, Texas Instruments
Pasi Tamminen, Nokia
Matti Uusimaki, Nokia
Joost Willemen, Infineon Technologies

B.0 Introduction

Several important issues for ESD/EMC/EMI have been discussed in detail and efficient methods for protection against these effects have been offered. Both ESD and EMC qualification requirements for electronic parts from various fields in the industry have been outlined. While all of the requirements must be met for the present state-of-the-art systems, the continuing trend in the scaling of silicon technologies is certain to place additional constraints on how effective ESD/EMI/EMC protection can remain. Limitations can come from various directions; it is likely though that new trends may alleviate these limitations to some extent based on future development and actual applications. These issues need to be examined in the context of future road maps.

B.0.1 Scope

The purpose of this appendix is to address changing technologies from different points of view that would have an impact on the near-term (2012-2022) design capability for system level ESD protection.

We will specifically cover integrated circuit technology roadmaps and trends, with consideration given to the system level ESD performance of:

- IT, communications, and automotive electronics.
- IC Package technology development and roadmap
- Advances in board and assembly technologies
- Advances in interconnects such as optical interconnects
- Advances in new suppressive materials such as polymers for IEC protection

A final objective of this appendix is to assess the impact of rapidly advancing technologies on system level ESD requirements and designs.

B.0.2 Background

The purpose of this appendix is to address changing technologies from different points of view that would have an impact on the design capability for system level ESD protection. In this context, we plan to address only the issues that would have an impact in the immediate future. Despite consideration for system level ESD, advancements in the electronics industry will continue to include scaling of IC technologies, new IC package development, and new consumer applications. Each advance has to be examined with a proper perspective to see where the IEC protection can be included or whether there will be a significant impact to on-chip protection from these developments. We review these trends for the selected topics and offer a view of how they might affect the future of IEC system level ESD.

B.1 Roadmap for ICs: Microprocessors

B.1.1 IC Technology Development

Continued scaling of silicon technologies is necessary for achieving higher speed circuit demands and higher density chips. Both White Paper 1 [1] and White Paper 2 [2] have reviewed these technology advances and have established the impacts on component level ESD targets. 3-D transistors like FinFETs [3] can have a serious impact on ESD sensitivity, but this is most likely limited to component ESD. Products built with advanced technologies which have applications in a system can effectively have an impact on the overall system performance. Thus, the impact from scaling in most cases comes directly from the sensitivity of the interface pins. Technologies in production now are at the 40 nm process node, with the 28 nm node under broad deployment, the 22 nm currently in production and the 14nm node under development (2012).

B.1.2 New Functions

As IC technologies continue to be scaled down, newer functions continue to evolve for achieving greater speed and performance. Some of the most important functions for IOs are high speed serial links known as SERDES macros. At the 40 nm node, SERDES operating frequency has been established at 12.5 Gbit/s, and soon will be at 15 Gbit/s for 28 nm and progressing to 20 Gbit/s at the upcoming 20 nm node. Similarly, double data rate (DDR) applications also have a high demand for speed: 1.5 G at 40 nm to 2.3 G at 28 nm. Fortunately, these SERDES and DDR pins are not system interface pins, and hence are not restrictive for IEC protection designs. In contrast, high frequency and high speed pins such as USB and HDMI can have direct interfaces and thus can pose severe challenges for IEC protection design. The same challenges also apply to RF Antenna pins that would have a direct interface while having low tolerance to capacitance from external protection devices.

B.1.3 USB Requirements

The roadmap for USB evolved from 12 Mbit/s (USB1) to 48 Mbit/s (USB1.1) and to 480 Mbit/s (USB2). The extension of USB frequency in the next few years will be to 5 Gbit/s for USB3. This is shown in Figure B1.

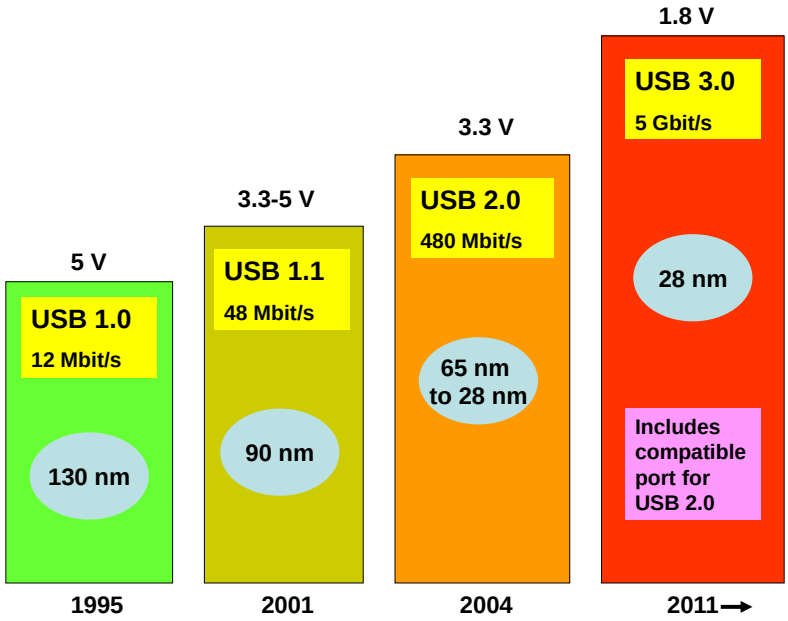


Figure B1: Trends in USB applications and data speeds. The insets represent the respective technology nodes of introduction (Courtesy of TI/Nokia)

At the present time, applications for USB 2.0 require meeting IEC protection challenges. These USB receptacles interface with IC pins that can often shunt at least 2 A of ESD current in the 100 ns regime as part of their component ESD protection. Thus, the board design to meet the IEC stress levels is not difficult as long as board components such as common mode filters (CMFs) are effectively used. There is always the question that if the USB 2.0 pins are recessed; do they really need IEC protection? Connectors for USB 3.0 would be an improvement, and thus might not face the same difficulty, but the higher speed of USB 3.0 would make it even more challenging to meet IEC protection. With USB 3.0, the interface to USB 2.0 would still be needed, and thus the same challenges would remain even if future applications switch to USB 3.0. But if customers demand IEC protection for USB 3.0, simultaneously meeting the frequency requirements of 5 Gbit/s versus designing for 8 kV IEC will require innovative approaches. In such cases, migration to polymer type protection might become necessary provided enough technical advances are achieved to make these materials practical for ESD applications.

B.1.4 HDMI Requirements

The roadmap for HDMI reflects a much more severe impact from new applications than for USB. Before HDMI, S-Video had been common but the S-Video data rates were slower. As the demand for high definition TVs has grown, HDMI data rates have increased from 1.8 Gbit/s to rates of 3.4 Gbit/s and higher. Eventually HDMI is expected to be replaced with Display Ports. These trends are indicated in Figure B2.

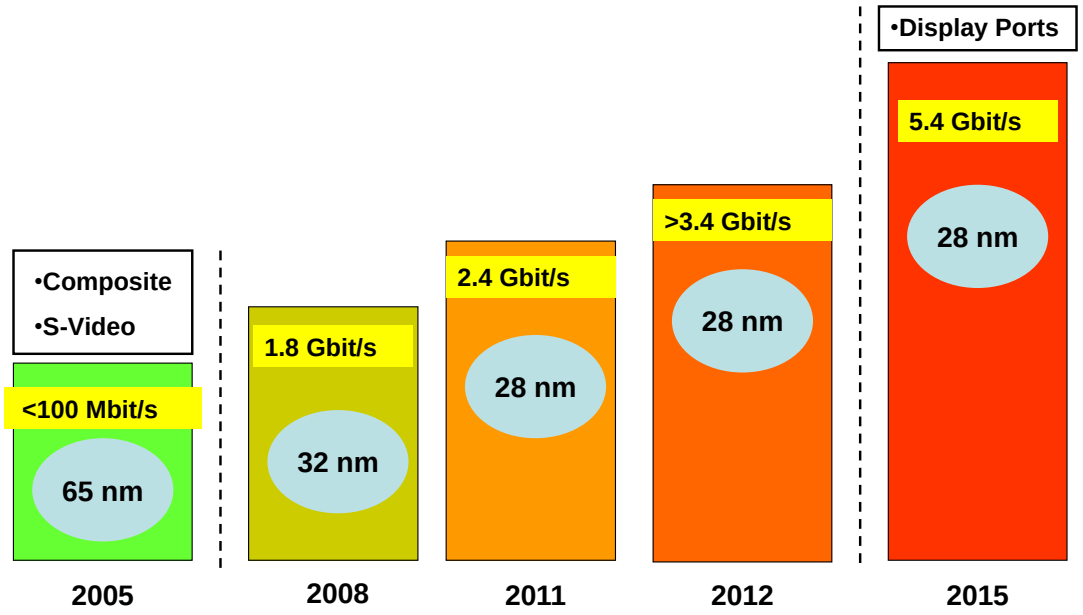


Figure B2: Trends in HDMI applications and data speeds. The insets represent the respective technology nodes of introduction (Courtesy of TI/Nokia)

It should be noted that Figure B1 and Figure B2 indicate that these speeds are achieved with 28 nm technologies whereas USB transfer rates of 5.4 Gbit/s have been achieved on 90 nm technologies and HDMI transfer rates of 3.4 Gbit/s have been achieved on 130 nm technologies.

The protection challenge for HDMI mainly comes from the intolerance of these interface pins to any value of series resistance larger than 2-3 Ohms. This is reflected in the relatively lower levels of component ESD performance for these pins (typically meeting only about 1 A TLP in the 100 ns regime). Moreover, as technology nodes shrink, the breakdown voltages at the IC pins are lower and thus the tolerable residual voltage at a particular residual current has to be smaller. This trend, combined with the fact that any board components such as a CMF or ferrite bead (FB) cannot be used due to their frequency limitations, requires the use of a very efficient TVS component (low capacitance, low breakdown voltage, very low on-resistance) to meet the IEC requirements. While this is possible to some extent today, within the next five years the problem will become much worse, and it may not be possible to meet an 8 kV requirement for HDMI at > 3 Gbit/s. Even if polymer ESD suppression components are to be used as a replacement for the TVS, the practical trigger voltages that would be available for these polymers would still make it difficult. Thus it seems that for the future, meeting expected IEC performance for HDMI could very well become a bottleneck.

B.2 Roadmap for Automotive Applications

B.2.1 Automotive Technology Trends

Automotive semiconductor products employ a variety of different IC technologies. The products made in the various automotive technologies have to be (a) robust in the harsh automotive environment (such as operating temperatures typically ranging from -40 °C to 175 °C), (b) subjected to strict reliability and safety requirements, and (c) directly or indirectly powered from a car battery supply network, which is exposed to many electrical disturbances.

Modern cars contain on the order of 50 to 100 ECUs. Typically, in an ECU we can distinguish different functional blocks:

- Voltage regulators: providing stabilized supply voltages from the car battery supply.
- Actuator control outputs: controlling electrical motors, valves, displays, lighting.
- Sense inputs: measuring physical quantities in the car, such as velocity, pressure, acceleration, temperature, etc.
- Communication: data communication networks (LIN, CAN, Flexray) are used to interconnect different ECUs in order to distribute sense and control signals inside a vehicle.
- Microcontrollers: for digital processing of sense signals and actuator control signals for monitoring and safety control functions.
- Memory: one time programmable (OTP), random access memory (RAM), electrically erasable programmable read only memory (EEPROM), Flash: for storing status, embedded software, trimming set-points, etc.

Many automotive ECUs consist of most or all of the above-mentioned functional blocks. Since the introduction of ECUs in vehicles, we see an on-going trend to miniaturization and reduction of component count per ECU. This is combined with an improvement of driver comfort, fuel efficiency, safety, and an ever-increasing expansion of features.

Reduction of component count is realized by combining functional blocks into single integrated circuits. Depending on the chosen system, partitioning different combinations of functions is possible. For instance, system base chips can combine regulators, small actuator drivers, monitoring sense inputs, and communication functions on one IC. Full system ASIC components combine even more functions in a single IC. In the future, the trend for further integration of functional blocks and enhancing features is expected to increase. The choice between different partitioning options is decided based on cost considerations. A further trend for reducing component count is the system-in-package (SiP) option. Here, multiple ICs, fabricated in different technologies, are mounted inside a single IC package.

Automotive IC technologies can be classified into different groups. For each of these groups, different technology trends can be identified.

- Low integration, such as smart switches (power devices with integrated simple diagnostic functions such as over temperature protection). The products in this group are mainly used as high current switches and are usually self-protecting regarding system level ESD. A

cost reduction trend, while maintaining or improving the basic device characteristics, is expected for the coming years.

- Medium integration, such as multiple switches and power regulators. These technologies will see a cost reduction, combined with an increase in logic density. The products in this class are often used for switching large loads and thus are self-protecting to system ESD stress.
- High integration, such as System Base Chips and system ASICs. This technology class comprises bipolar-CMOS-DMOS (BCD) technologies. The present state-of-the art is in the 0.13-0.25 um feature size range. In the next 5 years it is expected that technology feature size will scale into the sub-100 nm range. The chip area required for system level ESD protection is not able to scale down at the same rate as the logic feature size, as the energy of the ESD zap defines the chip area required to divert the ESD pulse.
- Integrated sensor technologies, containing sensing elements for different physical quantities, combined with signal processing and communication functions. The expectation for the coming years is an increase of logic density and signal bandwidth.
- Microcontroller technologies. Here the present state of the art is in the 90 nm to 130 nm feature size range. In the coming years it is expected to scale down to the 65 nm and 40 nm nodes. At present, there are no specific system level ESD requirements for microcontrollers. However, it is expected that system level robustness will be required for certain pins (GPIO, analog digital converter (ADC) inputs) with external PCB-level protection measures.

B.3 Roadmap for IC Package and Applications

B.3.1 Background to Package Technologies

It is well known that rapid advances in silicon process technologies are essential to enhance IC performance limits. At the same time, newer circuit development techniques must be state-of-the-art for achieving the required high speed in the 10+ GHz range. These effects, when combined together, are already taking a major toll in the ability to meet the ESD protection design requirements. The third dimension to this negative impact for ESD design can come from large package size effects. Other features such as stacked packages are introducing further complexity to ESD design and testing.

Package advances are based on requirements of the different market segments [4]. For computer applications, these package advances boost performance. For consumers, package advances are most guided by price and robustness. For automotive and military applications, package advances are often driven by increasing temperature sensitivity and reliability. Each type of package is then designed and selected according to the application. This package evolution has progressed from the standard dual-in-line (DIP) packages to multi-chip modules (MCMs) and to flip-chips and stacked die or even stacked packages. The future will see wafer scale packages (WSPs).

Although not a primary consideration historically, during package development, attention should also be given as well to ESD impacts. The aggressive technological advances into newer types of packages might very well determine the achievable ESD performance for overall adequate reliability. Looking to the future, moving from ceramic to organic types of substrates (or even for substrates without a die) may create susceptibility to damage of the package interconnect.

B.3.2 Novel Packages

The trend towards stacked die and stacked packages, as shown in Figure B3, is already showing various effects on ESD. When two different die are interconnected within the package and the power and ground are commonly shared, the effect is minor. But when the IO pads on both die interface with each other and the chips have no common ground, the ESD current paths will involve traveling through these chip-to-chip bonds (for example from ground of one die to IO of another die) and these ESD paths must be understood through modeling and simulations.

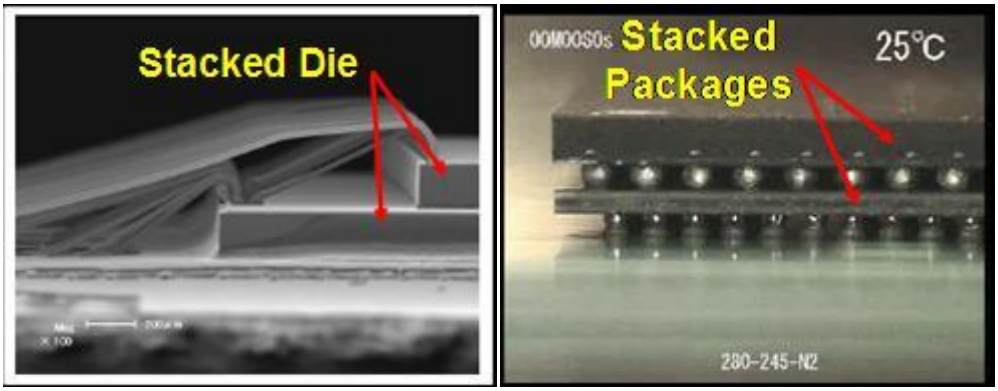


Figure B3: Stacked die versus stacked packages [4]

For stacked die packages, this can increase the complexity for ESD testing; therefore design methods must include analysis of the parasitic interactions between the die. Package development engineers are asked to develop new package materials to minimize the capacitance for large scale packages, and these new materials can have an ESD impact. Also, modeling is needed to understand the ESD current flow between die that have common bond wires and the inductive wiring effects for one package on top of the other.

B.3.3 System-on-Chip (SoC) and System-in-Package (SiP)

Novel SoC products continually require more features in a smaller space, and it is increasingly important that the power consumption, design time, and costs are optimized. SoC technologies help designers of these SoC products since they speed up system design when the core functions of the chip are well known.

SiP package developments (where multiple die stacks are packaged as a single unit) are evolving to the next phase of 3D devices involving connections using TSVs. In these cases the bottom die may have external connections while the power and ground connections are often shared among die stacks. The question then becomes what impact these new structures will have on system level ESD designs.

B.3.4 Applications with Impact on System Level ESD

A system design may contain several separate SiPs or SoCs from different sources, consequently the system designer needs to carefully match all IC and product interfaces. The matching phase includes EMC/ESD compatibility issues, as a single IC may contain for example, digital, analog and RF blocks. It may not be possible to separate noisy RF interfaces on a board from other

sensitive interfaces, and as a result, the board design gets more complicated. To improve on board integration and matching, more detailed information is needed from SoC blocks, and most likely early ESD/EMC simulations are needed to optimize the system design.

B.4 Advances in Board and Assembly Technologies

B.4.1 Changes in Board Technologies

Board technologies have evolved with new board construction materials and joint technologies. There will be more technology options, especially for high end, high mix, and low volume product areas. The existing surface mount technology (SMT) with FR-4 printed circuit boards will most likely continue to be the dominant board technology due to low price, high manufacturing capacity, and existing design tools. Low cost, high volume products will use these well tested board technologies, but they will use chips in advanced technologies. Very often high volume chips are made with the latest efficient silicon processes which will provide the best operations and cost efficiency. Combining traditional board technologies with novel IC and SoC technologies may bring challenges for the system design.

High end boards will use more complex constructions with anisotropic connection technologies, optical connections and flexible printed circuit boards. The base construction with these products will most likely be the basic SMT printed circuit board. Portable products with very thin designs will have electronic components distributed around the board. The design will get more complex when these distributed sub-components will be connected to the mother board through flexible cables and optical/electrical connections. These sub-assemblies may contain more sophisticated board technologies depending on the required function. Buried ICs and components in PCB cavities may be used to increase board integration. IC components will contain a number of functions and will eventually contain multiple chips in one package.

Board 3D design with stacked components, embedded components in PCB, SiPs, system-on-packages (SoPs) and other 3D constructions will be in the mainstream within coming years. There are also other special 3D designs like MID technology which may advance. In MID technology, a laser system writes the interconnect pattern onto an injection molded component from the computer aided design (CAD) data. This technology has been available for several years, but new laser and gluing technologies (isotropic conductive adhesive, anisotropic conductive adhesive and non-conductive adhesive) may speed the technology's advance.

A completely new high volume product family will be the R2R electronics as shown in Figure B4. These applications can combine passive and active electronics, optic and optoelectronic components, different indicators, sensors, and diagnostic products which are produced on paper, plastic foil or other more novel materials, onto a flexible medium. These products can be ultra-low cost and can be integrated into disposable products like a sales item package.

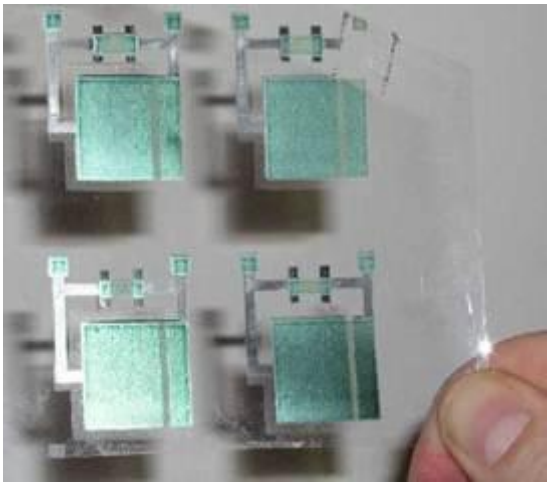


Figure B4: Roll-to-Roll electronics (Courtesy of VTT)

Printable electronics is close to R2R technology and can be used both with low volume and high volume areas. Printable electronics can be used economically to construct very low volumes due to low tooling costs. At the moment, these printable electronics products typically operate in lower frequencies and have lower reliability levels than conventional electronics. However, technology advances may enable high frequency solutions for printable and R2R electronics. Future manufacturing can employ nanoscale features which will be printed with Gravure inkjet printing, Flexography printing and Nanoimprint lithography. Advances with printable electronics rely mainly on the material technology development and how well the technology fits on a mass manufacturing area.

Board level interconnections will start to use nano/composite soldering processes such as shown in Figure B5. These new materials will improve interconnection strength, enable more dense joint connections, and may also decrease component package cost due to lower soldering temperatures. There is also development ongoing with board level conformal RF shielding. This can replace metal can shields, but will also pose limitations regarding reworkability of electronics.

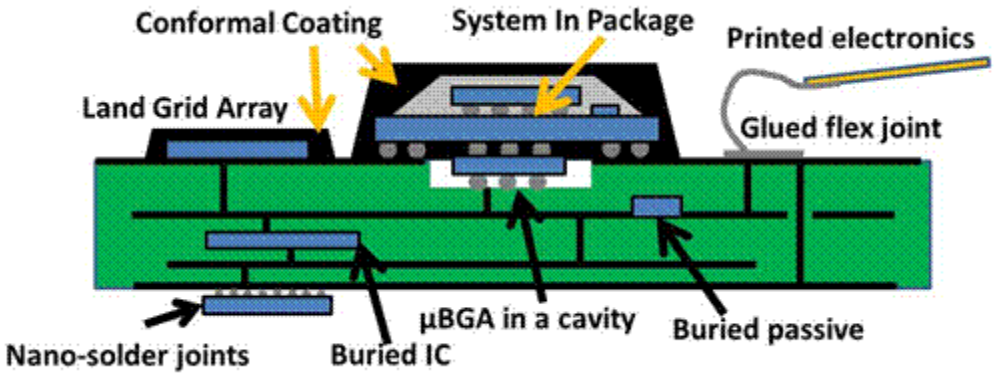


Figure B5: Board design with 3D designs, glued joints, buried electronics (Courtesy of Nokia)

All the mentioned advances in board and assembly technologies will have an impact on ESD and EMC design.

- The overall target of most of the changes is to decrease product dimensions and enable higher integration levels. From an ESD protection and EMC design point of view, smaller designs typically increase board signal coupling, crosstalk and interference challenges.
- Small physical design may limit system ESD robustness.
- On-board SiP and SoP components will have both interface and internal connections. There can be high level EMC noise in a chip when interface pins are stressed.
- Printable and R2R electronics will require both new design tools and also possible new EMC/ESD protection components which can be integrated into the new manufacturing processes.
- 3D designs require board designers to use simulation and modeling tools to optimize supply planes and signal routings due to a higher level of complexity.
- Components with very dense joint spacing require complex board designs where signal integrity and EMC issues will both need to be optimized.

Ultra low cost products will have additional challenges with ESD/EMC on new system designs. These products can also contain high-end technologies such as advanced SoC and SiP packages and high frequency connections. At the same time, the whole design must be made with the lowest cost. This requires using PCBs with only two to four layers, where common supply or ground planes may not be achievable. The amount of EMC and ESD filtering or matching components may also be highly limited to keep material costs down. Product physical designs need to be small, with covers and other mechanics designed for lowest cost. At the same time, the product may have the same design and acceptance targets from an ESD/EMC point of view as with high-end products.

B.4.2 Changes in System Boards

Technology advances will bring more functions to electronic devices in all product ranges. Advanced sensors (haptic control), high speed display technologies (3D displays), > 3 GHz data transmission, and optoelectronics will most likely increase system complexity. At the same time, product size, power issues, design time, and overall cost of design have very tight limits. These new systems on board will also be made with technologies which are not re-workable anymore (for example most glued joints cannot be repaired). This requires high quality design to reduce or eliminate risk of a re-design to fix problems in these areas.

B.4.3 3D ESD and EMI Effects

For stacked die packages, the complexity for ESD testing also increases and therefore the design methods must include analysis of the parasitic interactions between the die. Some basic structure analysis with simulations [5] indicates the importance of interposer design and the metal layer designs when stacking a couple of die together. When one starts to extend to several die on top of each other, the importance of bond wires and bond wire resistance/impedance becomes a dominant effect. The basic rule is to guide ESD and EMI energy back out of the component without traveling inside the component too deeply.

One of the complex issues for future technologies will be the EMI effects from stacking die [5]. As described in this reference, in the case of one or two die stacking, the dominant effect on EMI is the interposer design and die to die coupling. When there is more stacking, the bond wires become more and more important. That is, basically EMI effects depend on how the wires are implemented. In stacked structures, the proper grounding arrangement is the key. For example, if there is an EMC filtering die, it should be the bottom die of the die stack. Then, to minimize the ground impedance, grounding should be done with short bond wires. However, if the filtering die is on the top, there is extra ground impedance which creates unwanted ground bounce. Die to die coupling is very important. A basic EMC design rule is to guide the ESD/EMI out of the component as soon as possible. Going into future applications of die stacking, these effects could dominate the design of system level ESD.

B.5 Optical Interconnects

B.5.1 Introduction

Traditional metal interconnects within a die are rapidly becoming road blocks for RF speed and performance. To help resolve this issue, local RF wireless optical communications are being considered to communicate between chips on a circuit board, but these are typically only for special applications. It is expected that advances in optical interconnects will outpace those in conventional metal interconnects, and there will come a time when optical interconnects will be seen in all but the shortest and slowest on-circuit links [6]. Meanwhile, short distance wire connections will still dominate. As clock speeds increase, power efficient interconnection through metal wires becomes increasingly difficult. Thus, electrical signal interconnects will soon limit on-board communication between chips.

B.5.2 Impact on System to IC Interface

Once chip to chip optical interconnect becomes mainstream, it will also offer benefits for system level ESD. This is due to the fact there is no electrical coupling between ICs through signal lines,

so no ESD protection is required to the signal lines. This can be highly beneficial from a chip area perspective. However, at this stage it seems these technologies are still more than 5 years away from commercial use.

B.6 Polymer Applications

B.6.1 Need for Alternate Materials

While on-chip protection components can be designed to meet system level ESD requirements, they are definitely not practical due to their on-chip area requirements, and often may not consistently meet the specification requirements. These issues have been discussed in White Paper 3, Part I [5]. The design of on-chip IEC protection with compatibility to the circuit function is very difficult. For example, some external interface pins that require this system level protection may use SCR components, but these need to be free of latch-up issues during the stress. If an SCR component (which is very efficient) is used, its holding voltage at < 2 V it would not be compatible (without causing latch-up issues) for 3.3 V applications. Even if such large protection components are safely designed, they would require very wide (but impractical) metal widths to meet the current density requirements. Therefore, to effectively meet this stress challenge, an external protection method might remain as the only feasible approach.

The external protection components consisting of TVS components can be effective if the residual pulse entering the IC pin is compatible to its breakdown characteristic under transient conditions as outlined in the SEED approach. But with the USB roadmap, as described in Section B.1.3, the TVS component will start to have limitations. However, can we replace the TVS with polymeric materials? These polymers will be examined for their practicality.

B.6.2 Polymers

Polymer materials essentially transition from a nearly insulative state to a rapid conduction state with a response time of < 4 ps [7]. Their behavior can be understood to a first order with characterization using TLP. This is somewhat similar to the behavior of spark gaps but with two noticeable differences. In the case of a spark gap, when a high voltage pulse such as 1000 V is applied, the spark gap will allow the pulse to pass through without any clamping until it breaks down. But for a polymer, the voltage is clamped to between 200-400 V even before the polymer component breaks down. The second important difference between the two is the time needed to break down (statistical time lag). A spark gap can breakdown in as little as a few nanoseconds, but the polymer will first turn on in the picosecond to nanosecond range. Thus, the polymer will only allow a pulse of less than 1 ns and passing through 200-400 V while the spark gap will let a pulse of at least a few nanoseconds at 1000 V pass through. After breakdown both components have approximately the same clamping voltage of 25-50 V.

Systems will require a polymer designed/rated for the highest voltage used in the system, or at least used on a given PCB, and consequently may not be suitable for protecting low voltage pin applications (sharing the same PCB) that likely need most of the operational benefits that polymers offer (such as allowing for less capacitive loading ESD clamps on chip). Whereas engineering the polymer for the low voltage applications does not guard against the high voltage analog nodes from "triggering" the polymer's breakdown voltage during fast switching. If everything operated on the same (relatively) voltage, then this is not a problem, but such a scenario is not necessarily common in analog IC applications.

B.6.3 Polymer Impact on System to IC Interfaces

While it might appear that polymers are not suitable for low voltage applications, where the IC component breakdown values are typically in the 5-7 V range, the clue to its effective integration would depend on the manner in which the polymer goes into rapid succession of increasingly conductive states, thereby shunting the current away from the IC pin. At the same time as the IEC stress current is increasing, the on-resistance of the internal component may allow even more current to go through the polymer under breakdown. This type of efficiency, with these desirable qualities, would still require more research into making these materials while achieving good control, and allowing matching to the particular application.

Meanwhile, for higher voltage applications, polymers can offer immediate applications. As an example, for GaAs components, the breakdown voltages are in the 200-300 V range and thus a polymer in parallel can effectively protect them for both component HBM and the system level IEC stress. Other applications include micro-electrical-mechanicals (MEMs) with similar breakdown voltages.

How would implementation be done in the above applications? Integration onto the system board can be possible with a surface mount connector. Another approach uses an interposer board that will have the polymer matching the ball pattern of the IC. A third approach is to build custom PCBs with embedded polymer. Beyond that, the package integration of the polymer is under exploration.

B.6.4 Expediency for Board ESD Applications

ESD protection components have a number of characteristics (on-resistance, triggering and clamping voltage, capacitance, turn-on speed, leakage current, linearity, price, size, availability, etc.) and any requirement for ESD protection typically involves some tradeoffs to get an optimal solution. For example, polymer ESD suppression components typically have low capacitance, which is a desired feature for high speed signal line protection. However, polymer components also have the limitations of higher leakage currents after ESD pulses, and some of the polymer components also have relatively high on-resistance during ESD events. Polymer technology can provide reasonable ESD protection in many applications, but most likely polymers will be used along with other on-board protection methods (such as varistors, diodes, ferrites, and passive discrete components) depending on the required protection and signal integrity level.

B.7 Future Compatibility to IEC Protection Requirements

Part of system level ESD/EMC validation is the IEC 61000-4-2 stress tests. Here a system is stressed with up to 8 kV contact discharge and 15 kV air discharge. The same requirement is also increasingly being requested by suppliers for component qualification. It has been common to request up to 8 kV for those IO pins that may be stressed in a system. ESDA WG5.6 has created the HMM standard practice document to specify a corresponding system level test method at the component level. One option for this test is based on the IEC pulse waveform applied with an IEC “gun” (150 pF / 330 ohm circuit). In addition, a TLP-based pulse source can also be used for this component testing.

There are several open questions related to component level testing with IEC waveforms.

- Is the IEC current pulse a realistic stress waveform for a component pin which is on a board inside a system?
- Since the IEC pulse has been shown to have a wide variation in current and energy levels according to the standard, what is a "correct" stress level?
- Is there variation between the different ESD generators, both in the low frequency content and in the static behavior – how do we deal with this?
- How can possible component EMC/EMI related challenges be evaluated on a test board which differs from the final product?
- How much of the ESD pulse energy should dissipate within the IC, as system mechanics and board design will always have an effect on the final stress levels?
- New SiPs will typically contain interface connections. These components can be made with advanced wafer processes, and building up a high on-chip ESD protection level in these processes can be both challenging and costly.

Electrical products also vary in size from a small coin size battery operated electronic component up to a car size system. Small products can have a very high capacitance when tested on a test bench during IEC qualification while some products with a large plastic housing can be more or less electrically floating on a test bench. In the floating case, corresponding component ESD stress levels in the system can be totally different between different designs with the same initial voltage stress level. This can lead to both under- and over-estimations of the real component stress levels.

This raises the issue of whether it is beneficial to try to validate electrical components with similar setups and pulse waveforms as those delivered in a system qualification. Instead of trying to estimate the component behavior with IEC pulses, it could be more efficient to try to measure component operation and robustness during different stress situations. This data could be used by the system designer to build up required shielding and filtering for the component to withstand ESD/EMC stress in a system.

B.7.1 Impact of the Microprocessor Roadmap

Advances in microprocessor technologies will continue to pose a tremendous challenge for system level IEC robustness if the required and expected protection levels remain the same. The challenge of system ESD robustness comes at the expense of meeting the speed performance requirements for USB and HDMI. This raises the question of whether there should be new development for connector techniques, such that the ports are exposed for IEC zap tests. As these applications cannot rely on on-chip solutions, the use of external clamping needs to be more effective and relatively more efficient than what is commonly practiced today. One example of a solution could be the application of polymers. As long as the need persists where applications of these pins requires testing of the exposed entry points, innovation will continue.

B.7.2 Impact from the Automotive Roadmap

In the automotive industry typical maximum requirements for system level ESD robustness involve packaging and handling tests. System level testing for automotive applications is done with components connected to the cable harnesses with an 8 kV IEC requirement (contact

discharge) for automotive electronic control units. However, there is no universally required ECU system ESD level test, and the requirements differ from customer to customer.
The 8 kV target value is historically defined. In some cases, it is empirically determined in the laboratory by increasing the zap level until failures that appear in production could be reproduced. This has led, for instance, to the 6 kV requirements for transceiver pins from German OEMs [8]. At the moment, no trend to change from 8 kV contact discharge as a typical requirement is to be expected.

One method of system level testing is to test the system in the unpowered state. Minimum pass/fail testing involves monitoring of post-stress leakage currents at the stressed pins to detect IC damage. Improved pass/fail assessments are done with functional retesting after system level ESD zaps.

The importance of system level testing in the powered state will increase in the future. In this case, transient latch-up (TLU) events due to ESD zaps can also be detected. ESD zapping in the full functional state, as is possible at the completed ECU level, is not feasible on individual components. This, however, is required to detect possible ESD induced system upset.

At the moment, automotive OEMs are not aligned to support the recommendations of lowering HBM and CDM levels to 1 kV and 250 V, respectively. Their concern is that lowering HBM and CDM on local pins negatively affects the system level performance due to increased exposure to crosstalk between system level stressed PCB lines and neighboring board-internal traces, which they contend charge internal components and sensitize ESD current paths which can be tested by HBM and CDM.

The main challenge for system level ESD in future automotive products is expected to be in the high-integration ICs (refer to Section B.2). Several aspects have to be considered here, for more details see reference [9].

- The crosstalk issue, mentioned above, must be resolved. This should happen both at the ECU board level as well as at the IC level. If a real crosstalk threat is identified, design guidelines and simulation methods should be developed to identify weaknesses early in the design phase.
- If the occurrence of harmful board-level crosstalk can be excluded on physical grounds, the HBM/CDM levels for ICs that have only local, ECU-internal, connections can be lowered.
- If on-chip crosstalk between high current carrying system level pins and other on-chip nets turns out to be a real threat, the present trend of making certain IC pins system level robust will change and move off-chip, PCB level protection measures will be introduced. This will help avoid the high current peaks flowing into a possibly sensitive IC.
- Shrinking the technology feature size leads to higher packing density and higher clock rates for logic circuit blocks. The on-chip system level ESD protection components will not shrink at the same rate since the required ESD component areas are correlated to the amount of energy to be dissipated, which stays basically the same.

- With advancing automotive technology designed into smaller areas, logic and analog circuit blocks will become more sensitive to ESD if they are indirectly connected to exposed system level pins (such as low voltage devices cascoded with high voltage devices). Here, greater design effort must be invested to provide secondary on-chip ESD protection measures. This poses a risk to increasing area requirements for ESD protection.
- Scaling technology goes hand in hand with a decrease in supply voltage and signal levels. Lower signal levels increase the susceptibility to EMC types of disturbances and therefore EMC caused by system level ESD zaps. Again, this is a possible scenario that contradicts the present trend to have more on-chip system level ESD protection and drives towards more board-level protection.

New system level ESD test methods may become more prevalent in the future. For instance, with the LIN transceiver tests, defined by Volkswagen, a new indirect zap test has been introduced. In this test method, an IEC 61000-4-2 ESD pulse is applied to the shield of a coax cable whose inner lead is connected to a LIN terminal. This setup leads to an indirect coupled pulse on the LIN pin. The test is a novel way to emulate LIN bus line ESD response inside a vehicle chassis, which was identified as a source for destructive ESD coupling in some cases.

It is expected that comparable test methods may be defined in the future, in order to assess the ECU functionality on a test bench during qualification, before testing the ESD robustness of the completed vehicle.

In any case, the effectiveness of the new ESD test methods must be carefully assessed in order to optimize, and not to unnecessarily increase, the number of test methods. Careful studies of reproducibility, ESD generator dependence, occurring waveforms, calibration methods, sensitivity to changes in the setup, and other factors must be carried out before introduction of new test setups.

B.7.3 Conclusions from Technologies and IC Systems

There is strong competition in the system market. Here, the speed of component, system, and software design plays a major role in the electronics business. ESD and EMC design is one small part of the big picture, but it is critical to avoid non-optimal, unrealistic target levels or test methods which hamper technological advances. Arbitrary fixed stress levels, qualification standards, and targets will only create unnecessary conflicts between the component and system manufacturers. To avoid these conflicts, we need to verify that each component or system qualification and validation method provide useful information for the next technology advancement.

One future scenario could be that system manufacturers would leave behind all component ESD requirements, but request information on the component behavior and tolerances during different stress situations. Component suppliers would include this information and simulation models in the datasheets. In this case, the system designer could select the component based on parameters which best fulfill the need, and use SEED simulations to optimize the design and verify the system robustness with final stress tests.

B.7.4 Cost of System Level ESD Design

At present, there is confusion regarding whether the system designer (customer) or component designer (supplier) should bear the cost of ESD design for the system boards. Combined with this confusion is the pressure of time to market to deliver the product for applications. One OEM comments that time to market is a primary factor for system designers with low cost category products. For this category of products, the price constraints do not allow assignment of numerous EMC/ESD designers to achieve safe and effective solutions. Therefore, OEMs ideally want delivery of an IC with built-in IEC protection, ready for board implementation to improve confidence in the board level IEC protection.

This scenario means the cost shifts to the IC manufacturer. However, IC development costs could be very high if trying to meet the speed requirements with the extra load (resulting from requirements of system ESD immunity) in a large on-chip protection device. In the case of critical pins such as high speed USB / HDMI interfaces, this is not practical – that is, the on-chip solution approach is not acceptable. This means either more effective, shielded connector pins have to be developed or novel on-board solutions have to be created. Polymeric materials are one example.

What about the use of more "commercial packages"? System designers may be buying certain IC and layout designs for a specific purpose, such as the assembly of a simple mobile phone in just a few days. For these quick systems there would not be much room to squeeze in the EMC/ESD design components. So these challenges would continue into the future. All of the above point to an urgent need for constant dialogue between the IC supplier and the system board designer for each product / application.

References

[1] Industry Council on ESD Target Levels, "White Paper 1: A Case for Lowering Component Level HBM/MM ESD Specifications and Requirements," August 2007, at www.esda.org or JEDEC publication JEP155, "Recommended ESD Target Levels for HBM/MM Qualification", www.jedec.org

[2] Industry Council on ESD Target Levels. "White Paper 2: A Case for Lowering Component Level CDM ESD Specifications and Requirements," Revision 2, April 2010, at www.esda.org or JEDEC publication JEP157, "Recommended ESD-CDM Target Levels", www.jedec.org

[3] H. Gossner, C. Russ, J. Schneider, K. Schruefer, T. Schulz, C. Duvvury, R. Cleavelin, W. Xiong, "Unique ESD Failure Mechanism in a MuGFET Technology," IEDM Tech. Digest, pp. 101-106, 2006.

[4] D. Edwards, "High Performance IC Package Design and Electrical Reliability," EOS/ESD Sympoisum Proceedings 2003, pp. 1-7

[5] Industry Council on ESD Target Levels, "White Paper 3 System Level ESD Part I: Common Misconceptions and Recommended Basic Approaches," December 2010, at www.esda.org or JEDEC publication JEP161, "System Level ESD Part I: Common Misconceptions and Recommended Basic Approaches", www.jedec.org

[6] David Miller, "Rationale and Challenges for Optical Interconnect to Electronic Chips," Proceedings of the IEEE, Vol. 88, No. 6, June 2000, pp. 728-749

[7] M. Uusimaki and A. Renko, "A systematic Approach and comparison of different 3-D chip structures for electromagnetic compatibility" IEEE 0-7803-8443-1/04, 2004 IEEE International Symposium on EMC, pp. 734-739

[8] Based on emperical evidence coupled to the German OEM requirements and through personal communication with M. Hell, Infineon Technologies

[9] http://www.esdforum.de/Files/Impact%20of%20Lowering%20the%20ICHBM%20Robustness.pdf

Appendix C: Fast and Slow ESD Stress (High and Low Frequency Spectrum)

Matti Uusimaki, Nokia

C.0: Discussion

In ESD design at the product level, one should understand that there are several different phenomena involved. The first thing to understand is that there are two parts to an IEC 61000-4-2 ESD pulse; fast and slow ESD. The fast ESD stress refers to the high frequency content initial current pulse and the slow ESD stress refers to the low frequency content current after the initial current pulse. The fast and slow currents tend to use different current paths to ground. Current will always flow preferentially through the lowest impedance path. The impedance of any current path is, however, frequency dependent. Current paths dominated by capacitive elements will have their lowest impedance at high frequencies, while current paths dominated by inductance will have their lowest impedance at low frequencies. It is therefore not surprising that the initial current spike in the ESD waveform with its high frequency components may travel through a different path than the later parts of the ESD stress which is dominated by lower frequencies. See Figure C1 for more details.

As an example, in Figure C1 there is a large metal sheet which is grounded only at one end and floating throughout the rest of the area. Also shown in the figure is a simplified parasitic circuit element drawing for the mechanical structure (in dotted lines). Clearly visible is a capacitive and inductive path for the ESD current. In Figure C1, there is a fast stress capacitive path through the small board which can either overstress the components on the small board or could generate unwanted operation effects. The slow stress flows through the inductive path to board ground.

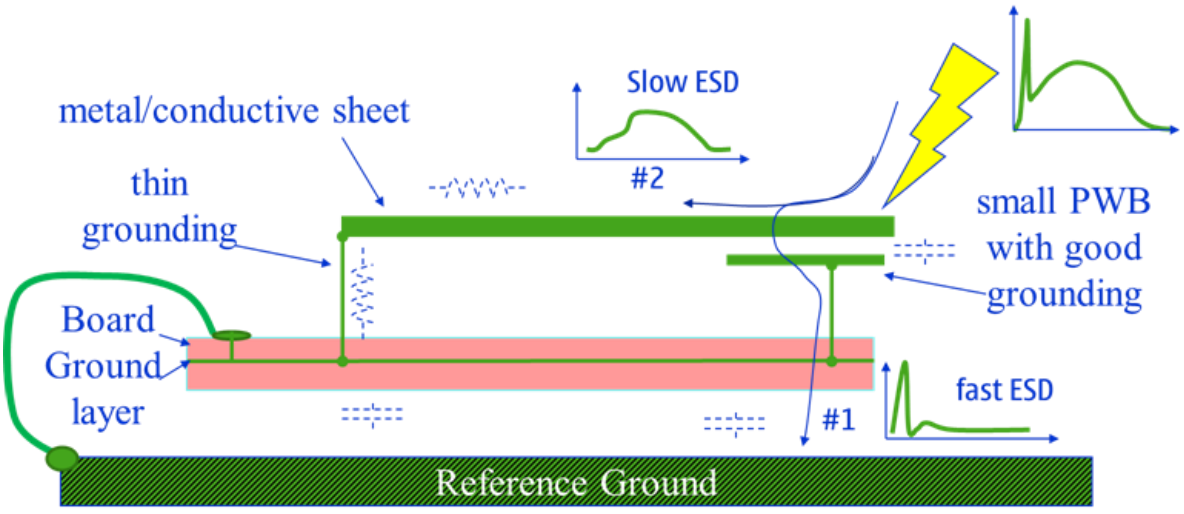


Figure C1: Fast and slow current ESD paths

For corrective actions, the ESD current flow needs to be redirected. In Figure C2, some options are shown:

C2a: Adding better grounding to all the metal corners can redirect the ESD current in a different path. This will reduce the high frequency impedance of the inductive path creating less fast capacitive ESD current coupling to the small board.

C2b: Add an additional metal shield over the small board. This will guide the fast ESD current to the main board and ground without disturbing the small board.

C2c: Improve the pig-tail grounding (i.e. reduce the inductive impedance) and additionally try to increase the connection impedance of the small board to the main board by adding coils or ferrites. However, in this solution, note that the impedance should be added to all lines. As a consequence the small board would "float" from an RF perspective, making the component more sensitive to RF fields. This solution needs careful tuning and should not be the primary fix.

C2d: Create some additional mechanical structures to introduce other current paths for the ESD pulse. Again, this is not as good a solution as proper shielding, but may work in some cases with proper fine-tuning.

Figure C2a: Good overall grounding

Figure C2b: Small board's own shield

Figure C2c: Better grounding, while increasing the impedance of the small board grounding. Note that this solution makes the small board more sensitive to other RF noises.

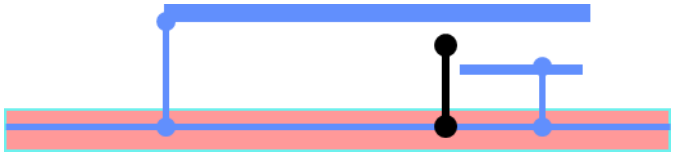


Figure C2d: Create an additional mechanical "ESD trap" to guide ESD for an alternative route.

When completing the ESD design, it is good to remember that ESD has a rather high momentary current. Let's look, for example, at Figure C3 in which the upper metal sheet is actually a printed circuit board and the thin pig-tail grounding is still in use. Assume, for example, that the high frequency impedance (inductive reactance) of the pig-tail is equal to 1 Ohm. If an ESD pulse creates an 8 A fast ESD peak current which sees the impedance of inductive reactance this will create a momentary 8 V (up to) ground bounce on the upper board, meaning the whole upper board voltage level will rise relative to the lower board reference level. Any sensitive signal connected between the boards with these pig-tails will have a momentary glitch in the signal between the boards. The example values given in these calculations are just relaying the idea of the phenomenon, not describing it in exact detail where the time effect should be addressed in more detail.

In this case, the best option is to have a differential signal transmission between the boards which has higher immunity to such ground bounces. However, the differential signal needs to have high enough swing with good drivers and receivers to minimize the noise effect. It is also a good idea that the logic connected in such interfaces is not asynchronous nor edge triggered. Level triggered (synchronous logic) is more immune for momentary glitches. That should be valid for all signals, including a reset signal for example. Reset signals are often edge triggered so small glitch can cause unwanted resets. There are use cases where an immediate reset is important or necessary for application, but if possible, some minor glitch filtering can be a good idea. This glitch filtering would of course need to balance the need between speed and sensitivity to small noise glitches.

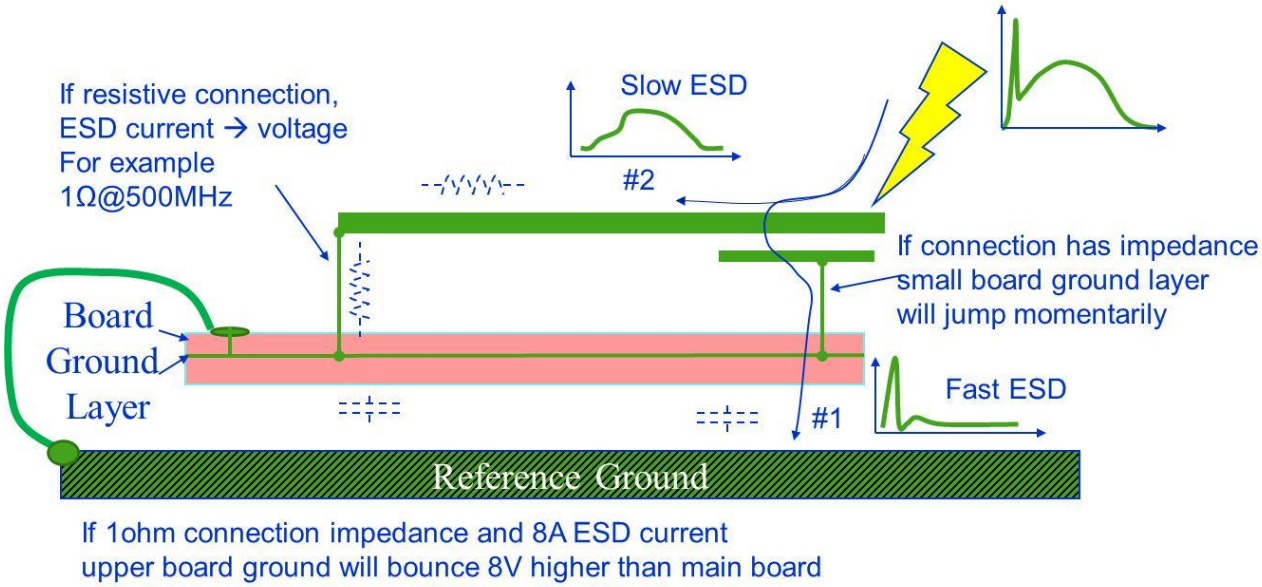


Figure C3: ESD current causes ground bounce

C.1: Some Words on ESD Debugging

In thinking through the ESD effect, one should remember that there are both ESD current and ESD voltage involved. The majority of the problems come from ESD current, but there are cases where ESD voltage (through the associated electric field) can cause a problem also. For example, a floating trace with weak pull-up or pull-down can cause edge sensitive logic to react to ESD noise induced voltage on the gate input. In the worst case scenario (Figure C4) the logic will react before the ESD event, just due to the charged ESD gun. In such cases shielding of traces and improving the pull-ups or pull-downs will help.

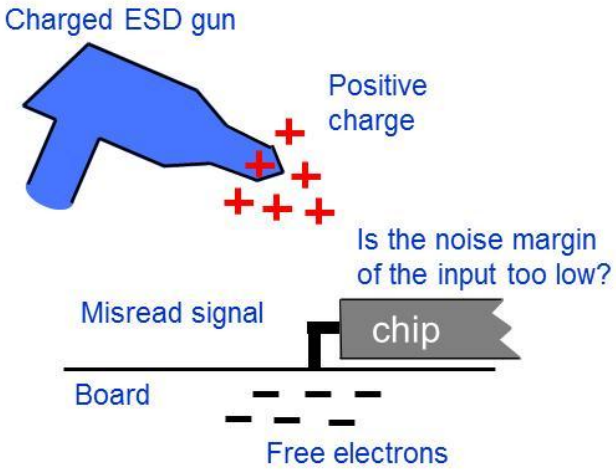


Figure C4: ESD induced noise on signal

A charged ESD gun (or some other charged material) can affect the board and could cause unexpected voltage levels on floating traces. All traces should be pulled to some known status. Also, all the unused IC IO pins should be set to an output mode to avoid unnecessary interrupts due to floating IO inputs. These unexpected interrupts can cause problems in software.

Understanding the ESD current path will help dramatically during ESD analysis. For example rearranging the grounding points of components or board subassemblies during ESD testing can help debug ESD induced malfunctions by isolating areas where the effect is reproducible. Root causes are more easily identified when the susceptibility is localized to a small area of the system. The root cause and the associated local area or sensitive IC can be identified using susceptibility scanning in which strong, but local transient fields are produced by driving electric or magnetic field probes using a transmission line pulse generator or equivalent disturbance generators.

As an example of isolating an area, one could begin inducing ESD into the board grounded on one end as shown in Figure C3, and then move away from this point (increasing voltage levels and alternating polarity in multiple passes) until failures begin to appear. Then one could move the ground to the other end of the board and identify the robustness of the area around that point until a susceptible area is found. Ideally this procedure will identify a localized area (or set of areas) in the system where the susceptibility is obvious. At that point the root cause analysis of individual components and signals in the area can commence. Of course this procedure is mostly relevant to soft failures and upsets, since permanent damage during hard failures is readily apparent and isolated to a particular component.

Appendix D: Review of White Paper 3 Part I

Robert Ashton, ON Semiconductor
Charvaka Duvvury, Texas Instruments

D.1 Part I Chapter 1: Purpose and Introduction

Part I Chapter 1 introduced not only the motivations for the document, as discussed above but also some of the common terminology to provide a basis for the paper. The most important was the distinction between ***internal*** and ***external*** pins in a system as illustrated in Figure D1. Pins that connect between chips on a board will not need the same level of system ESD protection as pins that attach to a bus which connects between circuit boards within a system. Pins which go to a connector, such as USB port, would require proper external clamp design to protect against direct system level ESD stress events. By the same token, some purely inter-chip pins may require more protection or design care due to crosstalk with signal lines connected to external connectors or long wiring harnesses.

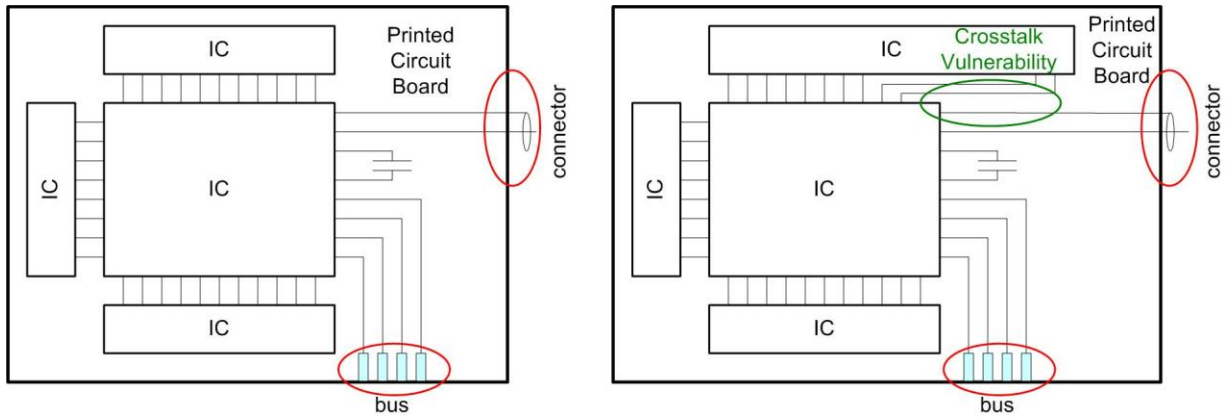


Figure D1: Classes of pins for specific system level ESD considerations including external and inter-chip coupling.

D.2 Part I Chapter 2: Test Methods and Their Field of Application

Part I Chapter 2 described how systems are tested for ESD with a focus on the most widely used standard, IEC 61000-4-2. This standard defines the stress waveform, the test environment and defines how a test plan should be developed. The IEC 61000-4-2 test bench is shown in Figure D2, showing direct stress to the unit under test as well as stressing to horizontal and vertical coupling planes which can induce errors due to coupling. The response to a system level ESD stress is not a simple pass/fail but has 4 levels of possible response as defined by IEC 61000-4-2:

a) Pass: Normal performance within limits specified by the manufacturer
b) Conditional Pass: Temporary loss of function or degradation of performance which ceases after the disturbance ceases. Equipment under test recovers its normal performance without operator intervention

c) Conditional Fail: Temporary loss of function or degradation of performance. Recovery requires operator intervention
d) Fail: Loss of function or degradation of performance which is not recoverable, owing to damage to hardware or software, or loss of data

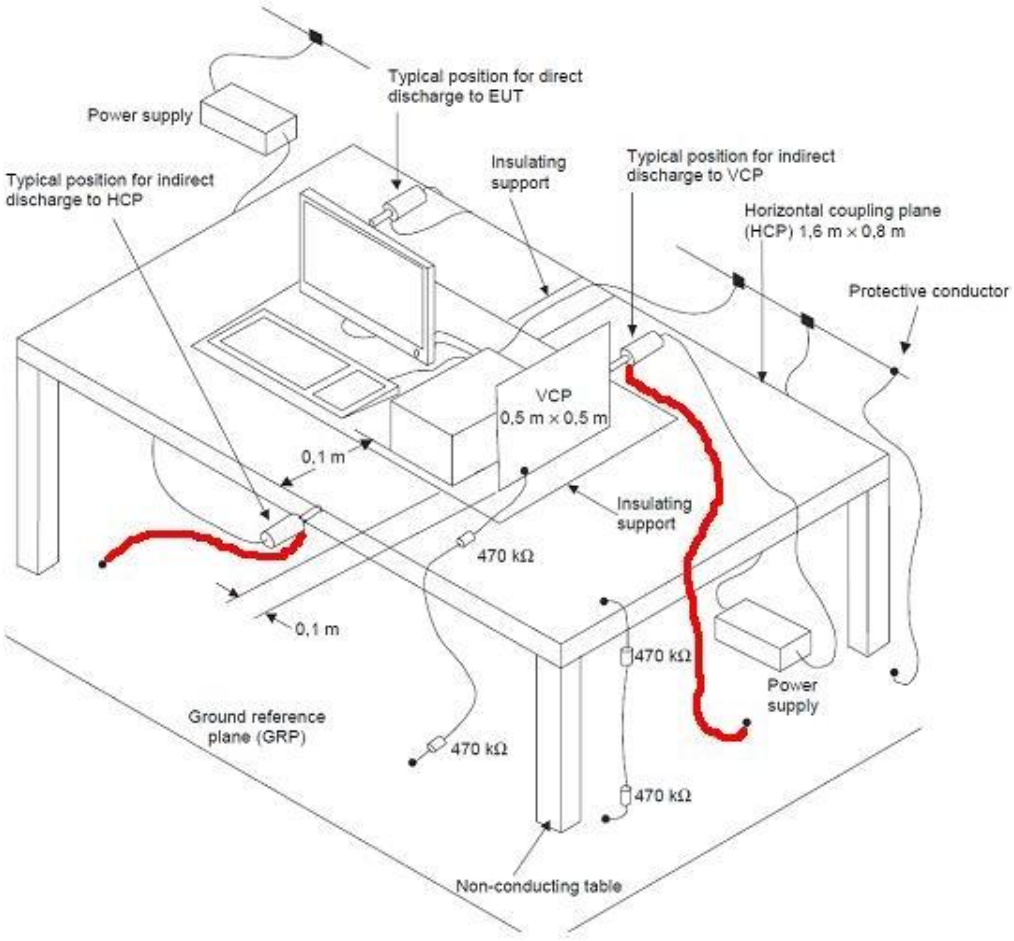


Figure D2: Test bench for IEC 61000-4-2 ESD testing [1]

Part I Chapter 2 also described several other system level standards that are based on IEC 61000-4-2, such as the automotive standard ISO 10605 and avionics DO-160 standard. The automotive and avionics test methods differ in detail from the more general IEC 61000-4-2, but the basic premises of the documents are similar and the failure modes are a combination of both recoverable failures and non-recoverable or hard failures. Chapter 2 also discussed two test methods in which system level ESD waveforms are applied to components. These include IEC 62228 for CAN bus transceivers and the more broadly applicable American National Standards Institute (ANSI)/ESD SP5.6-2009, which is known as the HMM. Both of these component ESD tests focus on physical failure and not system upset. It should be noted that IEC 62228 includes a suite of EMC tests other than ESD which do deal with system upset, however the ESD test does not deal with system upset.

D.3 Part I Chapter 3: Proven System Level Fails

Part I Chapter 3 presented analysis of 58 system level case studies provided by Council member companies. The type of failures and when the failures occurred are shown in Figure D3. The case studies cover the full range from system qualification, to field installation and field failure after installation. The types of failures include both physical and soft failures.

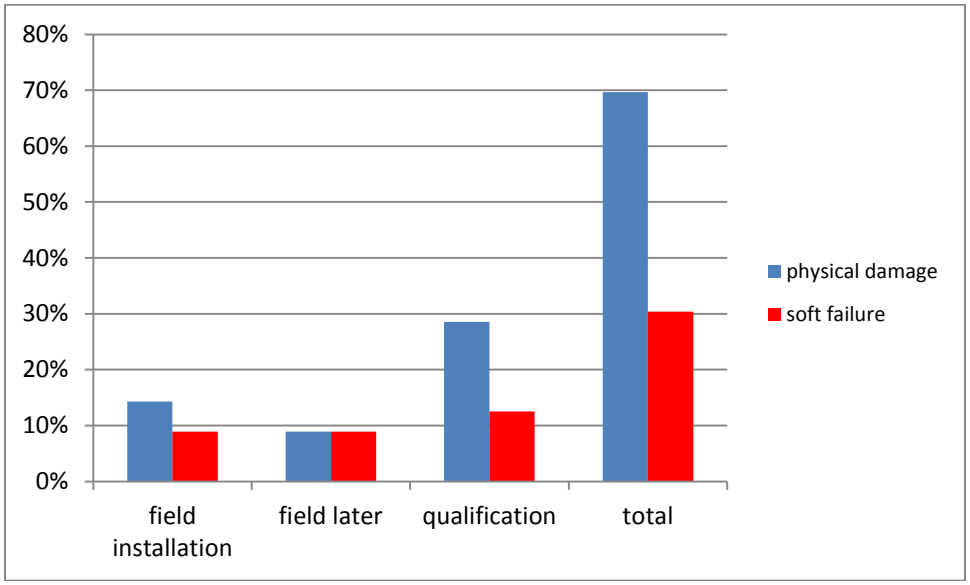


Figure D3: Types of failures and when failure occurred

How these problems were solved is shown in Figure D4. IC redesign was found to be the solution in only a small percent of the cases and that was only in cases in which the damaged pin was directly connected to a system IO. In one case, improving the HBM level of the IC actually resulted in a decrease in system level ESD robustness. The most interesting outcome of the case studies was that no correlation could be found between component ESD (HBM and CDM) and the system ESD failure levels of the products. Chapter 5 of Part I examined this in more detail in Section 5.1.5.

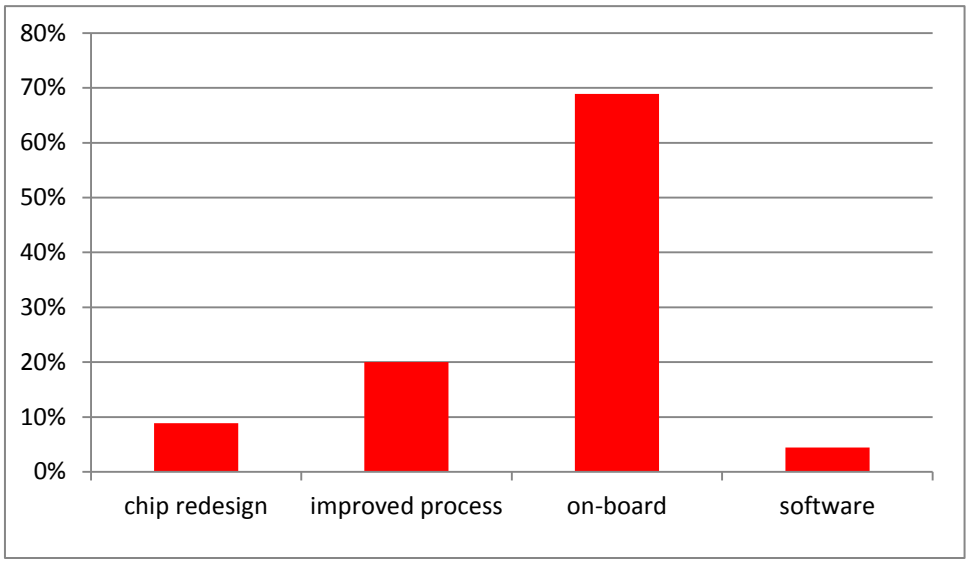


Figure D4: Solutions of system level failures

D.4 Part I Chapter 4: OEM System Level ESD Needs and Expectations

Part I Chapter 4 described OEM system level ESD needs and expectations. This chapter described three potential paths to designing ESD robust systems.

1. The components, including integrated circuits, chosen for the system are all inherently robust to system level ESD and the OEM does not need to think about system level ESD.
2. Not all components, including integrated circuits, chosen for the system are inherently robust to system level ESD, but component suppliers provide clear rules and procedures for using a set of system level ESD robust and non-system level ESD robust components that will produce an ESD-robust system.
3. Not all components chosen for the system are inherently robust to system level ESD, and the OEM has to find a solution on their own to design an ESD robust system.

The chapter then showed that Path 1, while appearing desirable, is not realistic for a variety of technical, practical and economic reasons. Path 3 is obviously undesirable since it is little more than a trial and error approach. Path 2 becomes the path of choice in which the properties of both ESD robust and non ESD robust components are understood and a design methodology is available to design a system with high probability of success. This path has been called system-efficient ESD design or SEED. This approach was described in the summary of Part I Chapter 6 and is a major topic of this white paper to be analyzed in more detail.

D.5 Part I Chapter 5: Lack of Correlation between HBM/CDM and IEC 61000-4-2

Part I Chapter 5 took on the question of correlation between HBM/CDM and IEC 61000-4-2 in detail. For the 58 case studies from Part I Chapter 3, only 9 were found to have both well documented HBM levels and system level data. The limited data in Figure D5 shows no evidence of a correlation between HBM level and system level ESD. The remainder of the chapter focused on reasons why a correlation between HBM levels and system level ESD should not be expected.

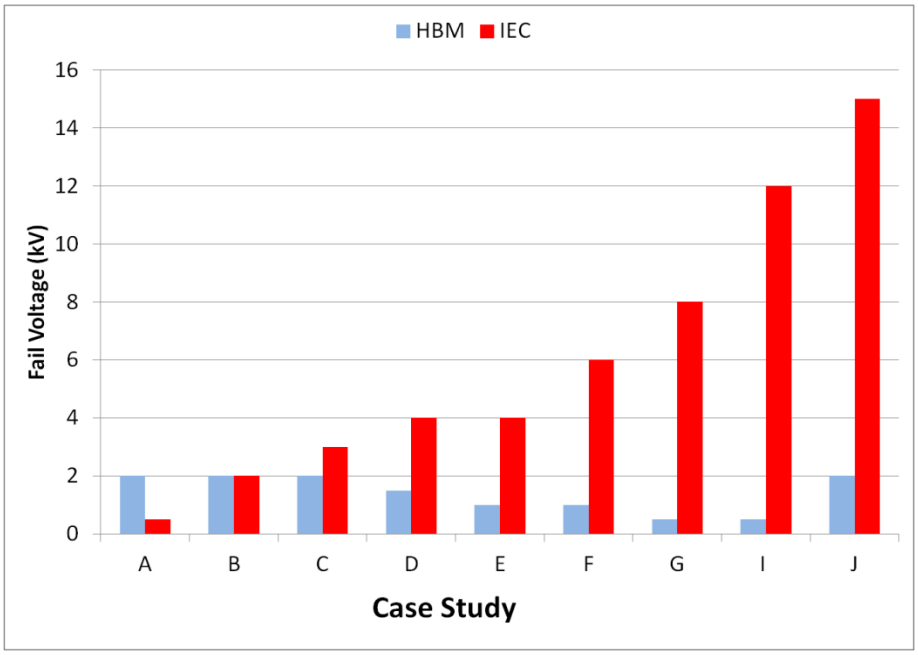


Figure D5: Component level HBM and IEC 61000-4-2 system level results compared

Component level HBM and IEC 61000-4-2 stress simulation circuit diagrams have a superficial similarity, but the waveforms are substantially different. HBM has a classic double exponential wave shape with a 2 to 10 ns rise time and 150 ns decay time constant, while the IEC waveform has an initial current spike with a sub-ns rise time followed by a second broader peak with a 50 ns decay constant. The applications of the two stresses are also totally different, as outlined Table D-1. With the major differences between the two stresses and the conditions under which they are applied, it was concluded that a lack of correlation in some cases was to be expected.

Table D-1: Comparison of IC level HBM (ANSI ESDA/JEDEC JS-001-2010) and System Level ESD (such as IEC 61000-4-2, ISO 10605)

	IC level ESD test	**System level ESD Test**
Stressed pin group	Multitude of pin combinations	Few special pins
Supply	Non-powered	Powered & non-powered
Test methodology for 'HBM'	Standardized	Application specific using various discharge models
Test set-up	Commercial tester & sockets	Application specific board
Typical qualification goal	1 ...2 kV HBM	8 …15 kV
Corresponding peak current	0.65 … 1.3 A	> 20 A
Failure signature	Destructive	Functional or destructive

Chapter 5 also looked for correlations in other system level tests such as CDE, transient latch-up (TLU), human metal model, extended length TLP, and CBE. While some correlations were found, such as between CDE and extended length TLP, no evidence could be found for higher levels of HBM or CDM leading to more robust system level ESD.

D.6 Part I Chapter 6: Relationship between IC Protection Design and System Robustness

Part I Chapter 6 dealt with the relationship between IC protection design and system robustness for physical, hard, failures by first introducing the concept of SEED. Subsequently this new concept was discussed in more detail and with specific examples. This involved detailed descriptions of a number of different considerations. IC ESD protection design methodologies were reviewed and it was shown that when the IC is included within a system, these methodologies are often not relevant to system level robustness. The chapter also examined the tradeoffs between adopting system level ESD protection within an IC (on-chip design) versus using board components (on-board design) for protection. On-chip system level ESD protection conceptually simplifies system design, but it significantly increases chip area and introduces on-chip protection techniques that are not always well suited for system level protection.

Full system ESD design was then introduced as shown in Figure D6. ESD stress can enter into a system by several paths, 1) stress to the system's cover creating ground currents, 2) stress entering through seams or vent holes, 3) stress entering through IO connections and 4) stress entering by arcs from nearby hardware such as screws in the system case. Of these paths, 1, 2, and 4 are best fixed by changes in the physical case to eliminate the stress. Only stress through a connector or to input/output devices, such as key pads, need to be protected by on-board or on-chip protection elements, or a combination of both. This is illustrated by the proper order of ESD solutions, a) cover redesign, b) air gap redesign, c) shielding and grounding, d) on-board protection and finally e) on-chip protection.

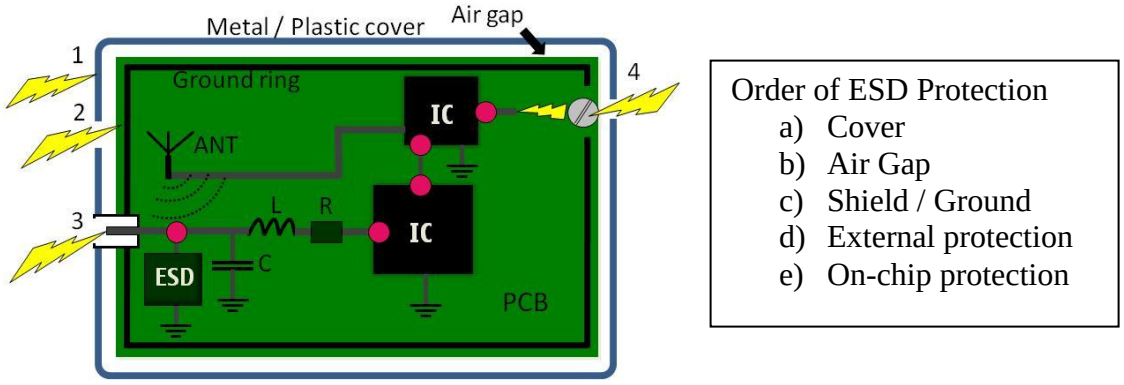


Figure D6: System ESD protection depends on product physical protection (covers), shields and groundings, on-chip and external signal protection and signal integrity targets.

There are several considerations for protection at the printed circuit board (PCB) level. On-board protection products including diodes, varistors and polymer components were introduced and the advantages and disadvantages of these products were compared. For protection of the most sensitive ICs, diodes have an advantage in terms of the balance of protection capability and minimal degradation in circuit performance. The chapter then introduced an overview of the SEED approach and its applications.

SEED primarily requires the understanding of the properties of the IC, on-board protection elements and the properties of the board and passive components on the board. This is illustrated in Figure D7. The properties of the IC and external transient voltage suppression (TVS) component are determined using TLP measurements. A standard 100 ns TLP system to mimic the long pulse duration (after the initial current spike) of the IEC stress pulse can be used. Knowing the properties of the TVS component and its response to the ESD stress, usually the IEC ESD waveform, it is possible to determine the residual voltage at the output of the TVS component. Applying this residual voltage in simulation to the IC, as filtered by on board components (such as resistors, capacitors, trace impedance, common mode filters, and chip ferrite beads), it is possible to determine the stress voltage and current which the interface IC pin actually experiences. If the calculated voltage and current are within the IC pin's safe operating area (SOA), the protection design can be considered acceptable. If, however, the voltage and current are outside of the SOA, either due to too high a current or too high a voltage, the protection design needs to be modified. This can be done in a variety of ways. A different TVS component can be chosen with lower turn on or lower dynamic resistance or the on-board components can be

modified to reduce the stress on the IC. In a more detailed analysis, as described in the chapter, the first spike of the IEC pulse may also need to be considered using very-fast TLP (VFTLP).

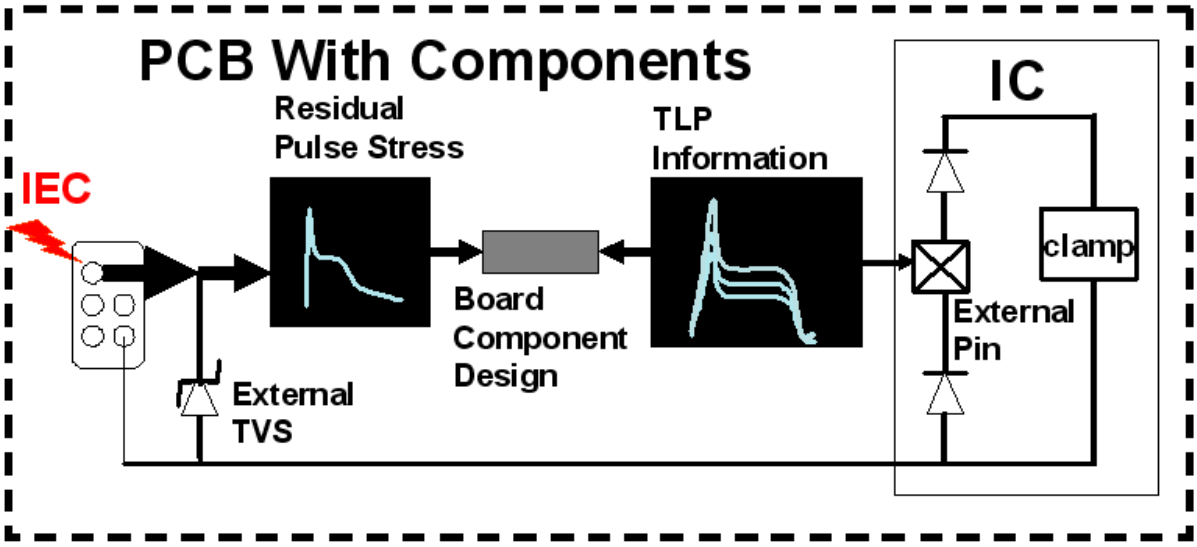


Figure D7: System-Efficient ESD Design (SEED) Methodology

D.7 Part I Chapter 7: Summary, Conclusions and Outlook

After reviewing the misconceptions about system level ESD and introducing a more realistic approach to efficient system level protection, the final chapter summarized the key takeaways from Part I. The summary of the method for producing successful system level ESD designs has the following key features:

- ESD test specification requirements of system providers must be clearly understood as a separate domain from IC level ESD specifications. IC level ESD specifications should not be used as a basis for system level requirements.
- Understanding ESD failure and upset mechanisms is critical to recognizing their relevance for robust protection design and for correlating them to the IC specifications.
- Most importantly, for achieving proper system level ESD protection, the responsibility must be shared between system designers and IC providers. This can happen only when a communication path is established for dealing with system level ESD design.

The document finally illustrated some product examples where, without this communication taking place, robust system level protection design could involve time to market delays and inefficient solutions. From the background information conveyed in Part I, the present document (Part II) examines more of these issues in greater detail and includes more details on soft failures for a more comprehensive understanding of system level ESD.

References

[1] IEC 61000-4-2, ‘Electromagnetic compatibility (EMC) – Part 4-2: Testing and measurement techniques – Electrostatic discharge immunity test’, Ed. 2.0, 2008.

Appendix E: Frequently Asked Questions

Q1: Why is the Industry Council addressing Non-Correlation issues between Component Level and System Level testing?
Answer: Some OEMs have been under the impression that higher levels of system robustness can be achieved by designing and measuring greater than necessary IC ESD levels. Our focus is to show that the system ESD measurement is relevant only when the IC is placed on the printed circuit board (PCB) and that stress data obtained at the IC level does not often correlate to system ESD capability when running the IEC 61000-4-2 test procedure.

Q2: Is there a correlation between component failure thresholds and real world system level failures?
Answer: There is rarely correlation between component (IC level) failure thresholds and real world system level failure in the field. Component failure thresholds are based on a simulated ESD voltage and current injected directly into the component (IC) with the component in a powered down condition. Real world system level failures in the field occur in many different conditions, most of which are powered. In addition, there is no clear definition of soft failure robustness for ICs, and many real world errors are soft failures. First one needs to establish reliable methods for soft failure evaluation of ICs before one can attempt to compare IC level and real world failures. In addition, system level ESD tests for hard and soft failures under operating conditions, while IC level mainly tests for damage under un-powered conditions.

Q3: *Why wouldn't you expect to see correlation between IC level and system level testing?*
Answer: Since the tests are done in different environments (unpowered versus powered or stand-alone versus on board) along with the different stress current wave shapes for the two tests, it is not surprising that they would be uncorrelated. In some instances external IC pins with higher IC level ESD robustness may result in less of a load on the board ESD protection components. However, there are many examples where an improved HBM level for an IC resulted in lower system level ESD as discussed in Chapter 5 and Chapter 6 of White Paper 3, Part I. The approach of relying on IC level ESD for system level ESD protection is not only impractical and unpredictable, it also detracts from the need for an efficient system ESD design in which the on board and on chip protection work together.

Q4: Can components really be designed to withstand real world system level events?
Answer: It is certainly possible to design ICs that can withstand system level ESD stress, but it is a complex and often unwise path. It is hard to know the exact details of the stress that will reach an IC on a board due to circuit board parasitics, making the design difficult and prone to overdesign. Additionally, IC protection for IEC stress consumes considerable area and is likely not to be the most economical path.

Q5: Do all pins on a component need to be tested using system level events?
Answer: External pins (such as USB data lines, Vbus line, identification (ID) and other control lines; codec and battery pins, etc.) need to be tested if the IC is not to be protected with on board components. But if the pin is to be protected by on board components, TLP characterization of the pin is more useful. Some internal ESD sensitive pins (such as control pins, reset pins, and high speed data lines, etc.) can be inductively coupled during a discharge to the case and/or to an adjacent trace of an external pin undergoing system testing. These pins need to be identified and may need to be tested using system level events.

Q6: If system level ESD testing at the IC level does not guarantee system level ESD performance, aren't higher target levels of IC HBM ESD better than nothing?
Answer: This would only give a false sense of security and could result in extensive cost of analysis, customer delays and a circuit performance impact. (Remember, higher HBM ICs may be harder to protect in a system!). System ESD protection depends on the pin application and therefore requires a different strategy. System level ESD is clearly important, but targeting excessive IC level requirements could pull resources away from addressing and designing better system level ESD.

Q7: Since ICs are now designed for lower IC ESD levels, why would this not be reflected by a sudden change in the overall health of a system for ESD capability?
Answer: The overall health of a system is dependent on a comprehensive approach to the protection methodology that includes a number of factors including on board protection components, optimized board signal routing, component packaging, mechanics (covers), and, as a last line of defense, the IC level protection.

Q8: How will you reach all the different system designers for their inputs?
Answer: The present document has been reviewed by a number of OEM representatives and they are in agreement with the conclusions of the document. We expect that the publication of this document will result in further input from the system design community.

Q9: If the system designers who are not involved in this document do not agree that it is a shared responsibility then what is next?
Answer: The system designers need to be educated in terms of system ESD versus IC protection design. Education with regard to these issues is a major focus of the Industry Council and we are convinced that as the benefits of the shared ESD responsibilities become evident more system designers will become convinced of their shared responsibility.

Q10: What is the purpose of IEC 61000-4-2?
Answer: The purpose of the IEC 61000-4-2 test is to determine the immunity of systems to ESD events during operation. The document states that it relates to equipment, systems, subsystems and peripherals, without further defining them. Its scope and description clearly indicate the purpose: to test electrical and electronic equipment that may be subjected to ESD from operators directly to the system under test or from indirect discharges from personnel to adjacent objects. See Section 2.0.1 of Chapter 2 in White Paper 3, Part I.

Q11: What is HMM?
Answer: HMM stands for human metal model. It is a method to assess the robustness of external IC pins against a system level ESD pulse. See Section 2.2.2 of Chapter 2 of White Paper 3, Part I for details.

Q12: Do all system level ESD standards use the same waveform?
Answer: In short: No. However, most use the waveform as defined in the IEC 61000-4-2, which is determined by a 330 Ω, 150 pF resistor/capacitor (RC) network. An example of a standard that uses a different waveform is ISO 10605. This standard uses the same type of ESD gun but the RC network is modified for some of the tests, using a 2 kΩ resistor and/or 330 pF capacitor instead of the values used in IEC 61000-4-2. See Section 2.1.1 of Chapter 2 in White Paper 3, Part I.

Q13: Is SEED considered to reproduce real, physical behavior of board and IC?
Answer: SEED is a concept to limit damaging current pulses reaching the internal IC pin. So in this sense it represents what the physical effect would be on the IC pin coming from an IEC stress at the external port of the PCB. What it represents for the board depends on how well the scenario is represented during the SEED analysis.

Q14: How can system/board designers get the required information about the IC IO behavior?
Answer: First, both the OEM and the IC supplier must define the 'external pins'. Following this, the IC supplier provides the TLP curve of the pin under interest with either bias applied or without bias which would depend on the pin application in the overall system board. The measured TLP at the pin will not only represent the pin's internal ESD clamp behavior but it will also include the IO design behavior to the transient pulse analysis.

Q15: What is the required degree of accuracy of the simulation models?
Answer: The simulation models can only be as accurate as the measured waveforms at the external clamp under IEC pulses along with the variations, and the internal IC clamp under the TLP conditions. Experience will teach us what level of accuracy is needed. Even if early attempts at simulation do not have the level of accuracy we may desire, the simulations will still provide insight into the ESD properties of a design.

Q16: Can the SEED concept ensure system robustness against any EMC and ESD related fail?
Answer: SEED is a concept to develop a robust system based on characterization of its components when subjected to IEC ESD stress conditions. There is a wide range of EMC type interferences and resulting fails. Established best practice EMC design approaches and quantitative analysis by simulation are not replaced by the SEED concept. Moreover, the robustness of the system against high energy pulses like an ESD discharge is built on the assumption that low amplitude interference can be handled by the system through appropriate EMC design.

Q17: Can I also use SEED for systems not listed in this White Paper?
Answer: Definitely. SEED is a basic concept which can be applied to any system. The main constraint is that all relevant components of the system have been characterized accordingly and modeling information is provided to the system designer.

Q18: OEM customers require specific system level ESD tests like (MM-like) bipolar testing. Do component suppliers need to satisfy both SEED characterization and additional company specific test requirements?
Answer: SEED is built on the knowledge of the failure mechanisms known by the large group of experts contributing to White Paper 3. It is the expectation that the SEED concept also addresses design optimization measures which will improve robustness against bipolar pulses. The requested tests are a matter of supplier-customer relation. Industry Council recommends the efficient test and design flow which is described within SEED.

Q19: White Paper 3, Part I introduced the concept of system-efficient ESD design (SEED) approach to system / component ESD co-design. Are there more details in Part II extending this SEED approach to other than "hard" system failures?
Answer: Yes. White Paper 3 Part I introduced the term system-efficient ESD design (SEED) by giving the basic example of a hard fail at an external pin. This has been expanded upon in White paper 3 Part II. SEED includes characterization and design optimization for hard fails at external pins, transient latch-up at internal and external pins and soft fails due to noise injection.

Q20: Can I apply the SEED concept right away for my products?
Answer: In principle yes, as long as the models and tools are available for the specific system. However, in practice there is still a ways to go. For example, both transient latch-up and noise characterization methods need to be defined in more detail and finally standardized. White Paper 3's main intention is to guide the industry towards developing the ecosystem to enable successful use of SEED.

Q21: In addition to the "hard" system failures described in White Paper 3, Part I, what additional failure types are described in Part II?
Answer: Beside irreversible hard failures, which exhibit physical damage of the component, so-called soft failures are also discussed. Soft failures are reversible by definition. These failures might require intervention of the user or the system could also exhibit a short interruption of normal operation and regain full functionality without intervention. Detailed definitions for hard and soft failures are given in Chapter 2. The document also provides a novel categorization of hard and soft failure types linking them to the underlying physical stress mechanisms and the applications of SEED (Chapter 4).

Q22: What are the most common ways external events happen and couple into a system?
Answer: External electrical events include ESD (Electrostatic Discharge), EFT (Electrical Fast Transients) from switching of inductive loads and running motors and nearby lightning (Surges) which are all transient effects and can also include RF (Radio Frequency) being radiated or conducted into a product. In this document we are only dealing with ESD. However, EFT is in many ways similar to ESD and can be coupled into a system in a similar manner. Further details on how ESD is coupled into a system are given in Chapter 2. Another way to categorize the way external events happen is by what the external root cause is: 1) a charged person discharges into a product; 2) a charged product discharges when it is plugged into a system; 3) a charge cable discharges a product and 4) a charged product discharges into another product when they are joined together in use.

Q23: Are there ways ESD / EMI can enter a system that is not well understood and modeled at this time? Does Part II describe these and provide guidance or direction for understanding?
Answer: While the physics of direct or indirect injection of charge into a system are well understood, it is hardly ever possible to model the complete entry path of ESD due to the complexity of real systems if both enclosure and PCB details are to be included in the same model. For example, it is very difficult to model the upsets of LCD displays including their control circuits and the direct coupling of ESD transient fields into those integrated circuits. However, the spread of ESD currents into a system can be modeled using EM simulators, and the propagation and absorption or reflection at ESD protection components and IC input can be modeled using SPICE simulators. Use of past experience, system component susceptibility and 3D case simulation where practical are all encouraged during system design. However, it is important to note that poor realization of a good design can break all design efforts to shield a system.

Q24: If I am developing a synthesized IC (with external IP) for system applications, what would Part II propose regarding how to investigate its system ESD susceptibility? Do simulation tools exist (or can they be developed) to investigate this?
Answer: Simulations tools (SPICE, VHDL-AMS, VERILOG-AMS, etc.) are capable of nodal analysis that can identify susceptible pins and/or internal circuits. However, these tools are only as good as the netlists and the models that they are provided as input. Often the netlists provided by external IP providers are focused on functionality and do not include the parasitic elements (for example, lateral or vertical bipolars in an IC's IO) nor do they model the high current regions of operation that are necessary for system ESD modeling.

Q25: How would troubleshooting a "soft" internal system failure differ from troubleshooting a "hard" failure? Does Part II give guidance on this?
Answer: Soft failures can be understood and fixed by three methods. The most common is trial and error in diverting the ESD current, shielding using ferrites or filtering of lines. A more in-depth method is to identify sensitive nets or ICs using susceptibility near field scanning which locally injects ESD derived noise into traces or ICs to determine at which level of local injection the same soft failure is observed as in system level testing. The third method uses software and firmware to identify which process or trace has been disturbed.

Q26: Regarding common shielding / isolation methods for improving system ESD performance, which method works best for soft failures? Does it depend on the type of soft failure?
Answer: At first one should determine which IC is affected, and in which traces or cable connection the noise couples. This is best done by susceptibility scanning the device for sensitive areas. After the sensitive nets, connections and ICs have been determine countermeasures such as improved field confinement of wanted signals, guiding of ESD currents, filtering of wanted signals, shielding or software changes can be implemented. Still, there is no simple solution for improving system ESD performance to reduce soft failures. In one case, shielding can be effective, but with another design isolation of a sensitive circuit might be effective. Use of shielded cables can certainly be effective but this is not always cost effective; isolating sensitive circuits may not be possible when the system consists of a single PCB with interfaces to the outside world. The type of soft failure depends on the system functions and which may be critical to operation. Chapter 3 contains information regarding the use of shielding to prevent ESD upset.

Q27: I have read that system ESD / EOS failures can result from isolation from / reconnection to ground. I know the IEC 61000-4-2 test provides for system testing of systems not having a path to ground. But this test passes on my system.
Answer: Regarding the ungrounded product which passes the IEC test: If during the test the product becomes charged an ESD event could certainly occur if some metallic part on the product suddenly becomes grounded -- by connecting a grounded cable or dropping it on a metal surface for example. If this is a concern, then an IEC test should be expanded to include discharging the product after a test.

Q28: Does EOS cause different system failures than system ESD failures? What is the difference?
Answer: This depends on the interpretation of the vaguely defined term electrical overstress (EOS). In the broad definition ESD is a subset of EOS. But often one uses the term more narrowly to refer to failures and damage due to transients of high power. Usually, the hard failures caused by a system level ESD will show less severity than an EOS due to a power transient. While ESD applies a limited pulse of stored energy to a component which may damage it during the short discharge pulse, EOS usually results from a condition where a component is subjected to a relatively large source of energy. As a result, when a failure occurs, EOS damage tends to produce extensive melting and charring at the damage location while ESD stress tends to leave burned junctions, blown oxides and melt stringers in its wake. The boundaries between ESD and EOS physical failure are not firm and some ESD, such as charged board events and cable discharge events have sometimes been initially mistaken for power-transient induced EOS. In some cases an ESD can trigger a subsequent stress such as latch-up, which may then appear more like an EOS.

Q29: Are there "non-invasive" methods of system board analysis for system ESD immunity?
Answer: Non-invasive methods for system level analysis are mainly software based. In many cases it is possible by reading register values, by checking bus errors, by looking for terminated processes to identify the root cause of a soft failure. This might require that the firmware is written with ESD soft failures in mind to provide sufficient error recording and register read out.

Q30: What board-specific design considerations in Part II will be useful to help reduce the incidence of "soft" system ESD failure? For example, placement of components, type of component used, trace isolation, shielding, etc.?
Answer: Primarily, all nets in a board design need to be grouped into nets which are connected to IO ports on the board, (nets connected to other boards or to system IO ports: HDMI, USB, etc.), nets that stay on the same board but have a high likelihood of coupling, and low risk (short, well shielded) nets. If available from IC soft error qualification, the sensitivity of each IC pin for all ICs on the board with respect to ESD-induced soft failures should be known. Those nets which connect to sensitive IC pins and that are connected by IO ports or have a high probability of coupling need to be filtered or rerouted if possible. Further, in software and firmware design, possible bit-error detection strategies should be considered to allow for transparent error recovery.
The enclosure design is a primary methodology for guiding the ESD current and the associated fields such that the coupling to the interior of the enclosure and to PCBs and board to board connections is minimized. Connector shells are typical entry points. These should be connected to the enclosure using a 360 degree connection. Even an inductance of 2 nH between a connector shell and an enclosure will allow a 5 kV ESD to create a pulse of about 35 V between the connector shell and the enclosure. This pulse will drive a current onto the PCB increasing the

likelihood of soft failures. The second aspect of the enclosure design is to avoid any non-grounded metal as these can cause secondary ESD.

Q31: From this white paper, are there test methods other than IEC 61000-4-2 that are relevant to understanding system level ESD failures?
Answer: The most common ESD scenario relevant to system level are the human metal discharge (IEC 61000-4-2), the discharge of cables which are plugged into connectors and the discharge of furniture, such as metallic lab carts. The discharge of cables is certainly of growing importance as these ESDs often lead to damage because the ESD currents can be injected directly into the pins of high speed interfaces. At present no tests are conducted for the discharge of furniture, however in the 1980's a "crossed vane" simulator was used. Experience showed that discharges from the IEC 61000-4-2 ESD generator at about 2-3 times the charge level provide the same failures as the crossed vane simulator. There is a plethora of application specific test methods that relate to system level ESD failures as described in Chapter 6. However, many of them refer back to IEC 61000-4-2 as specification of the stress waveform. Special ESD tests which are conducted for satellites are not covered by this white paper. Tests have also been developed, but not yet standardized for Charge-Board Events (CBE) and Cable Discharge Events (CDE). The ESDA is working on a CDE test method.

Revision History

Revision	Changes	Date of Release
1.0	Initial Release	September 2012